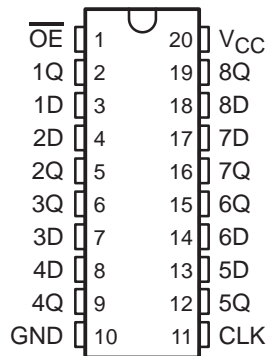


# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

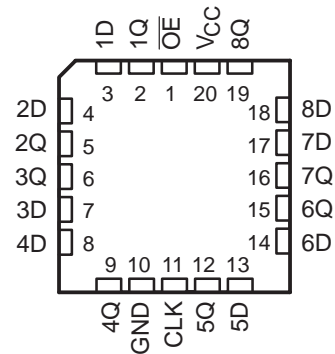
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- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

SN54HC374 . . . J OR W PACKAGE  
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC374 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HC374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	PDIP – N	Tube of 20	SN74HC374N	SN74HC374N	
	SOIC – DW	Tube of 25	SN74HC374DW	HC374	
		Reel of 2000	SN74HC374DWR		
	SOP – NS	Reel of 2000	SN74HC374NSR	HC374	
		SSOP – DB	Reel of 2000	SN74HC374DBR	HC374
		TSSOP – PW	Tube of 2000	SN74HC374PWR	HC374
Reel of 250	SN74HC374PWT				
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HC374J	SNJ54HC374J	
	CFP – W	Tube of 85	SNJ54HC374W	SNJ54HC374W	
	LCCC – FK	Tube of 55	SNJ54HC374FK	SNJ54HC374FK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

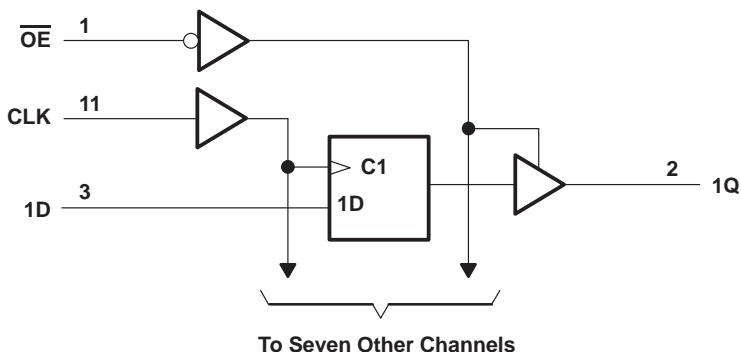
$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±35 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

		SN54HC374			SN74HC374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.5		0.5	V
		V <sub>CC</sub> = 4.5 V			1.35		1.35	
		V <sub>CC</sub> = 6 V			1.8		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V			1000		1000	ns
		V <sub>CC</sub> = 4.5 V			500		500	
		V <sub>CC</sub> = 6 V			400		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		6 V		±0.01	±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF



# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC374		SN74HC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency	2 V	6		4		5		MHz
	4.5 V	30		20		24		
	6 V	35		24		28		
t <sub>w</sub> Pulse duration, CLK high or low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t <sub>su</sub> Setup time, data before CLK↑	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		25		21		
t <sub>h</sub> Hold time, data after CLK↑	2 V	10		13		12		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	12		4		5	MHz	
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t <sub>pd</sub>	CLK	Any Q	2 V		63	180		270		225	ns
			4.5 V		17	36		54		45	
			6 V		15	31		46		38	
t <sub>en</sub>	$\overline{OE}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		14	26		38		32	
t <sub>dis</sub>	$\overline{OE}$	Any Q	2 V		36	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		16	26		38		32	
t <sub>t</sub>		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2 V	6	12			5		MHz	
			4.5 V	30	60			24			
			6 V	35	70			28			
$t_{pd}$	CLK	Any Q	2 V		80	230		345		290	ns
			4.5 V		22	46		69		58	
			6 V		19	39		58		49	
$t_{en}$	$\overline{OE}$	Any Q	2 V		70	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		22	34		51		43	
$t_t$		Any Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

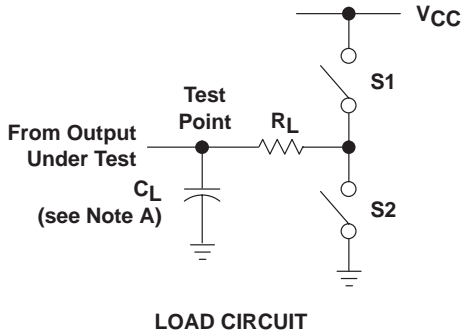
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per flip-flop	No load	100	pF

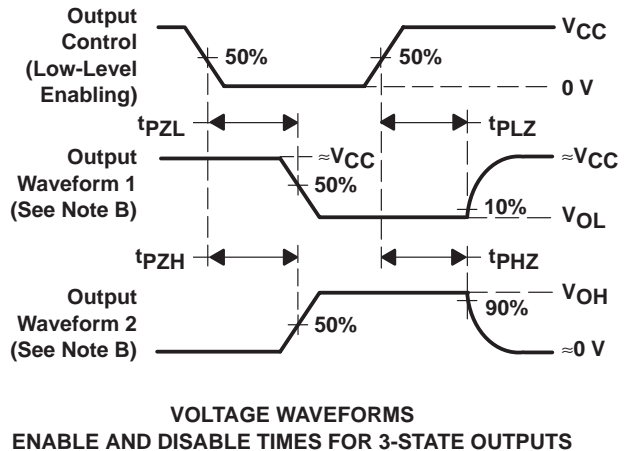
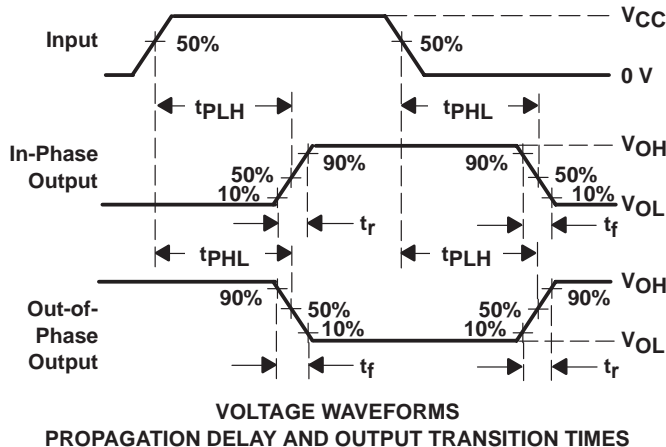
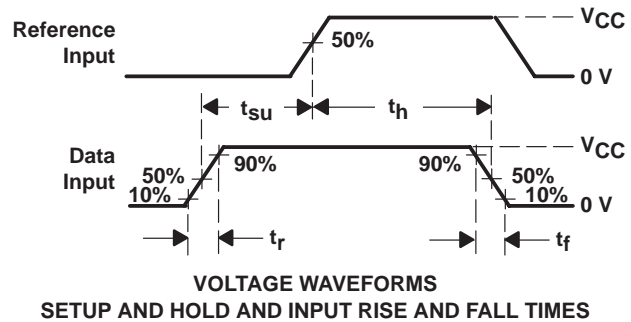
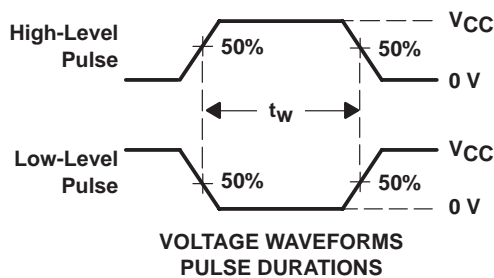
# SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 E. The outputs are measured one at a time with one input transition per measurement.  
 F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8407101VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8407101VR A SNV54HC374J	<a href="#">Samples</a>
5962-8407101VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8407101VS A SNV54HC374W	<a href="#">Samples</a>
84071012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84071012A SNJ54HC 374FK	<a href="#">Samples</a>
8407101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8407101RA SNJ54HC374J	<a href="#">Samples</a>
8407101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8407101SA SNJ54HC374W	<a href="#">Samples</a>
JM38510/65602BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65602BRA	<a href="#">Samples</a>
M38510/65602BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65602BRA	<a href="#">Samples</a>
SN54HC374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC374J	<a href="#">Samples</a>
SN74HC374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC374N	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC374N	<a href="#">Samples</a>
SN74HC374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SN74HC374PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC374	<a href="#">Samples</a>
SNJ54HC374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84071012A SNJ54HC 374FK	<a href="#">Samples</a>
SNJ54HC374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8407101RA SNJ54HC374J	<a href="#">Samples</a>
SNJ54HC374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8407101SA SNJ54HC374W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC374, SN54HC374-SP, SN74HC374 :**

- Catalog: [SN74HC374](#), [SN54HC374](#)
- Military: [SN54HC374](#)
- Space: [SN54HC374-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC374NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC374PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC374DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HC374DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC374NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC374PWT	TSSOP	PW	20	250	367.0	367.0	38.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

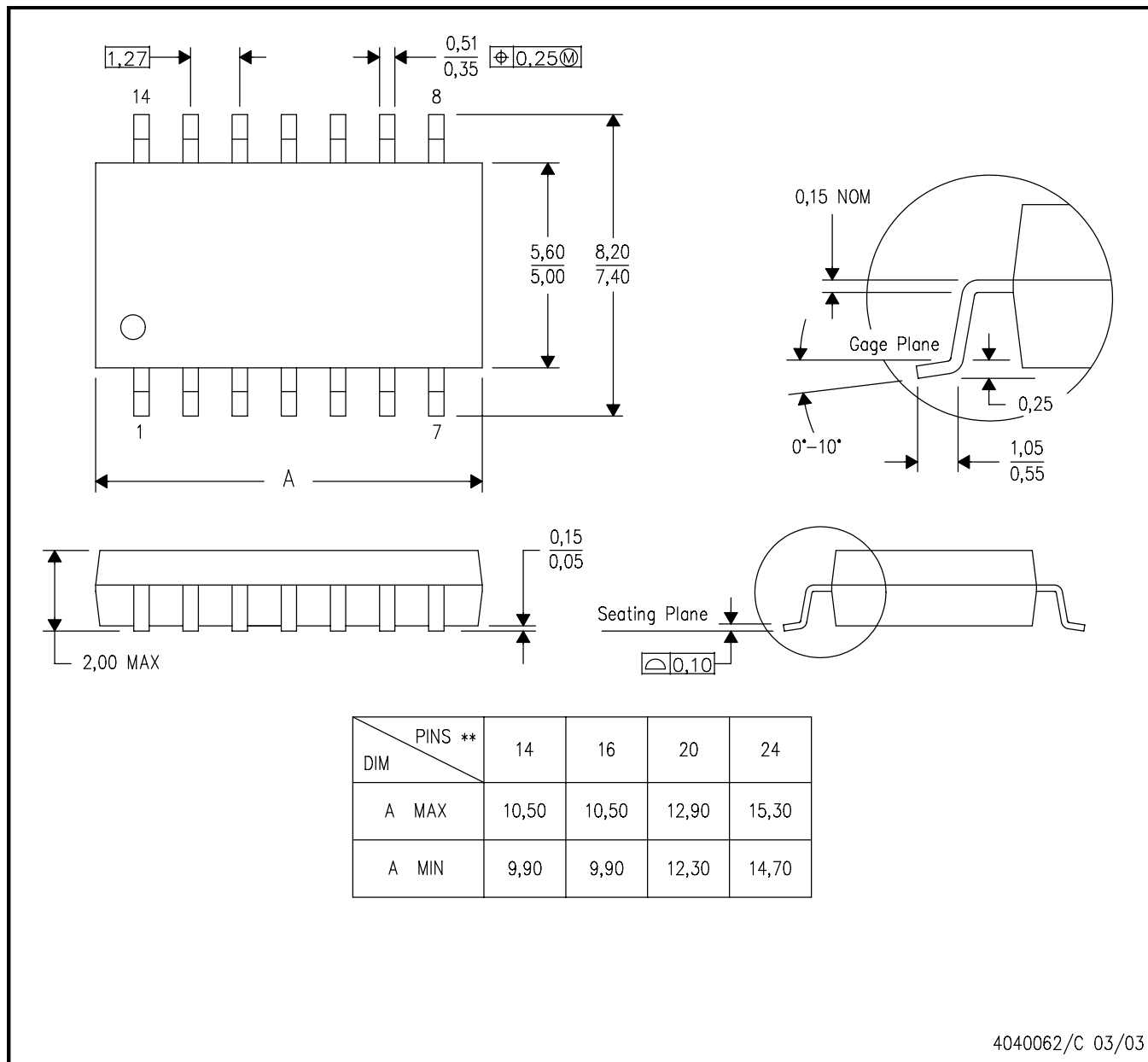
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

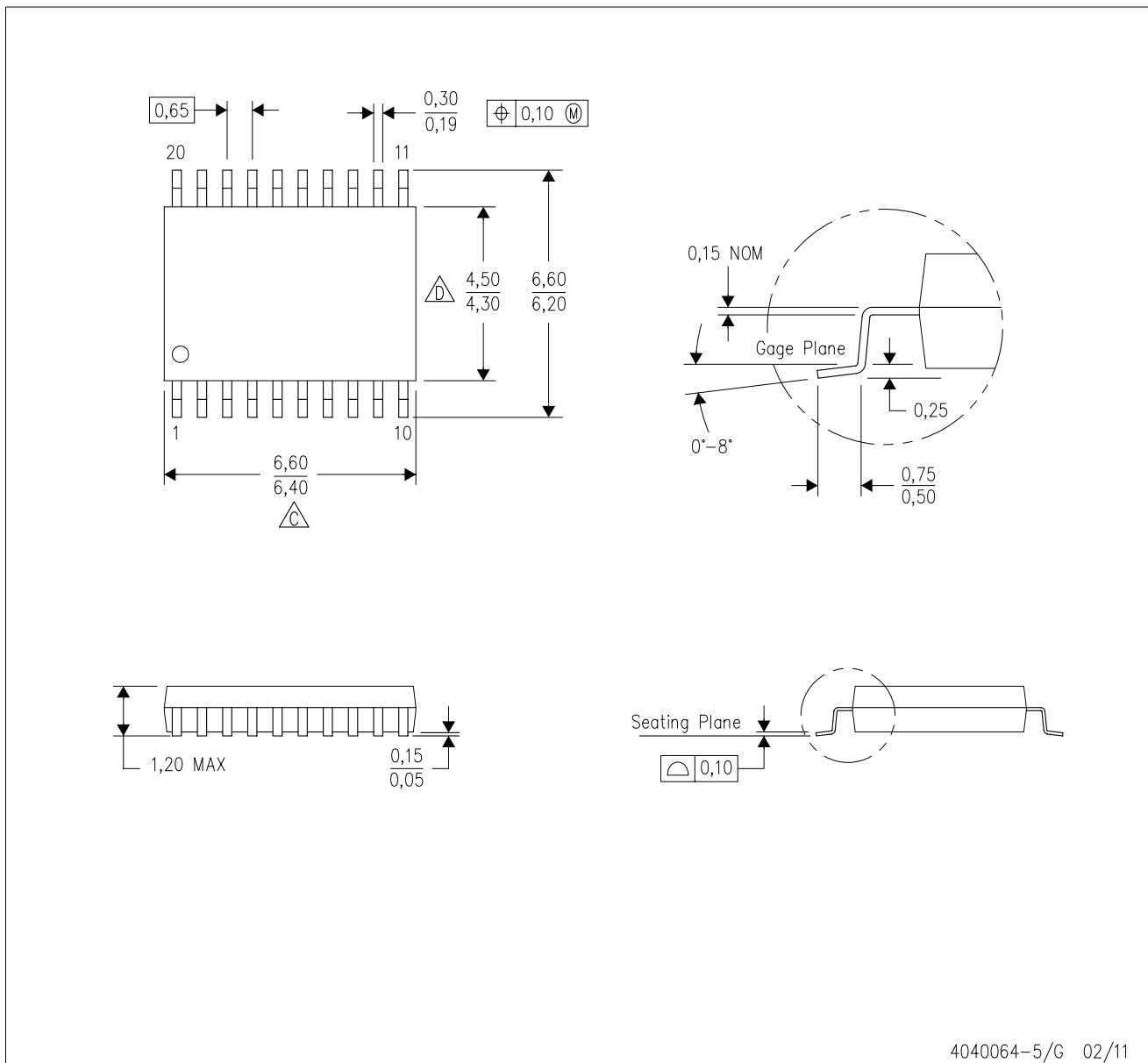


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

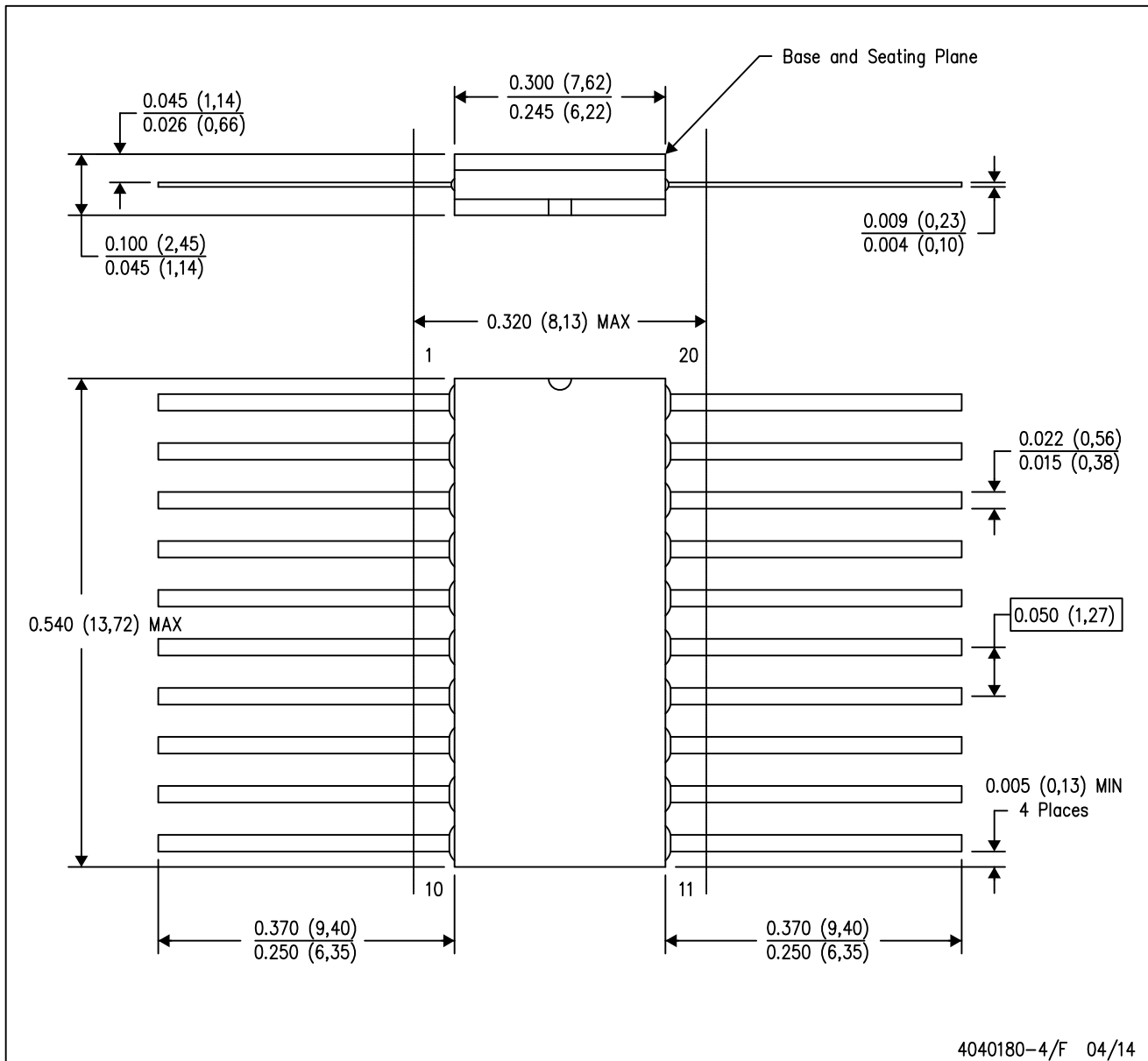
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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