Data Sheet

ADIN1100

Robust, Industrial, Low Power 10BASE-T1L PHY

FEATURES

- 10BASE-T1L IEEE Standard 802.3cg-2019 compliant
- Cable reach up to 1700 m with 1.0 V p-p and 2.4 V p-p
- Supports 1.0 V p-p and 2.4 V p-p transmit levels
- MDI polarity detection and correction
- Supports intrinsic safety applications
- Low power consumption: 39 mW (dual supply, 1.0 V p-p)
- Diagnostics
  - Cable fault detection with TDR
  - Link quality indicator with MSE
  - Frame generator and checker
  - Multiple loopback modes
  - IEEE test mode support
- MII, RMII, and RGMII MAC interfaces
- MDIO management interface
- Unmanaged configuration using pin strapping
- 25 MHz crystal or external clock input (50 MHz for RMII)
- Single or dual supply with 1.8 V or 3.3 V operation
- 3.3 V, 2.5 V, or 1.8 V MAC interface VDDIO supply
- Integrated power supply monitoring and POR
- EMC test standards
  - IEC 61000-4-4 EFT (±4 kV)
  - IEC 61000-4-2 ESD (±4 kV contact discharge)
  - IEC 61000-4-2 ESD (±8 kV air discharge)
  - IEC 61000-4-5 surge (±4 kV)
  - IEC 61000-4-6 conducted immunity (10 V/m)
  - IEC 61000-4-3 radiated immunity (Class A)
  - EN 55032 radiated emissions (Class B)
- Small package: 40-lead, 6 mm × 6 mm LFCSP
- Temperature range
  - Industrial: −40°C to +85°C
  - Extended: −40°C to +105°C

APPLICATIONS

- Process control
- Factory automation
- Building automation
- Field instruments and switches

FUNCTIONAL BLOCK DIAGRAM

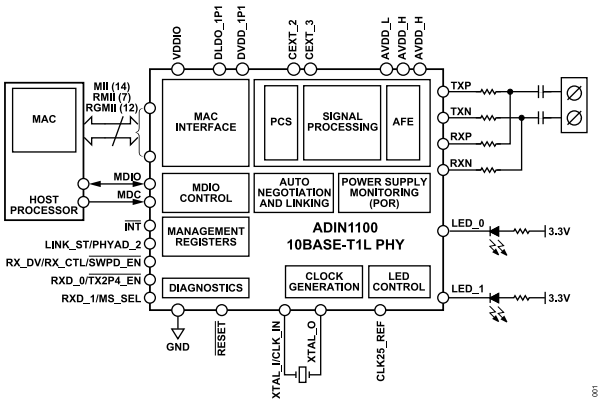

Figure 1.

GENERAL DESCRIPTION

The ADIN1100 is a low power, single port, 10BASE-T1L transceiver designed for industrial Ethernet applications and is compliant with the IEEE® 802.3cg-2019™ Ethernet standard for long reach 10 Mbps single pair Ethernet (SPE). The ADIN1100 integrates an Ethernet PHY core with all the associated analog circuitry, input and output clock buffering, the management interface control register and subsystem registers, as well as the MAC interface and control logic to manage the reset, clock control, and pin configuration.

The ADIN1100 supports cable reach of up to 1700 meters with autonegotiation enabled and has ultra low power consumption of 39 mW.

The PHY core supports the 1.0 V p-p operating mode and the 2.4 V p-p operating mode defined in the IEEE 802.3cg standard and can operate from a single power supply rail of 1.8 V or 3.3 V, with the lower voltage option supporting the 1.0 V p-p transmit voltage level.

The ADIN1100 has an integrated voltage supply monitoring circuit and power-on reset (POR) circuitry to improve system level robustness.

The MDIO interface is a 2-wire serial interface for communication between a host processor or MAC and the ADIN1100, thereby allowing access to control and status information in the PHY core management registers. This interface is compatible with both the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.

Rev. C

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REVISION HISTORY

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1/2023—Rev. 0 to Rev. A

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9/2021—Revision 0: Initial Version

SPECIFICATIONS

AVDD_H = AVDD_L = VDDIO = 3.3 V; DVDD_1P1 from internal low dropout (LDO) regulator (DVDD_1P1 = DLDO_1P1); all specifications at −40°C to +105°C, unless otherwise noted.

Table 1. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS/OUTPUTS					Applies to MAC interface pins, MDC, MDIO, $\overline{INT}$, LINK_ST/PHYAD_2, $\overline{RESET}$, and LED_x
VDDIO = 3.3 V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (minimum) = 2 mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (minimum) = 2 mA
VDDIO = 2.5 V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (minimum) = 2 mA
V_{OH}	2.0			V	I_{OH} (minimum) = 2 mA
VDDIO = 1.8 V					
V_{IL}			0.3 × VDDIO	V	
V_{IH}	0.7 × VDDIO			V	
V_{OL}			0.2 × VDDIO	V	I_{OL} (minimum) = 2 mA
V_{OH}	0.8 × VDDIO			V	I_{OH} (minimum) = 2 mA
$\overline{RESET}$ Deglitch Time	0.3	0.5	1	µs	
LED/LINK STATUS OUTPUT					
Output Drive Current			8	mA	VDDIO = 3.3 V
			6	mA	VDDIO = 2.5 V
			4	mA	VDDIO = 1.8 V
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I/CLK_IN pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−30		+30	ppm	
Crystal Drive Level		<200		µW	
Crystal ESR			60	Ω	
XTAL_I, XTAL_O Input Capacitance ($C_{IN,EQ}$)		1.5		pF	Equivalent parallel differential input capacitance looking into XTAL_I/CLK_IN and XTAL_O pins
Crystal Load Capacitance (C_L)[1]		10	18	pF	Including PCB trace capacitance and XTAL_I, XTAL_O $C_{IN,EQ}$
Start-Up Time			2	ms	Crystal oscillator only
Clock Input (CLK_IN)					
Clock Input Frequency		25		MHz	Requirements for external clock applied to XTAL_I/CLK_IN pin, media independent interface (MII) mode
		50		MHz	Reduced media independent interface (RMII) mode
Clock Input Voltage Range	0.8		2.5	V p-p	
Clock Input Duty Cycle	45		55	%	
XTAL_I Input Impedance ($Z_{IN,EQ}$)					
Driving Point Resistance (R_P)[2]		6		kΩ	R_P||C_P
Driving Point Capacitance (C_P)[2]		3		pF	
Jitter Tolerance (RMS)			40	ps	

SPECIFICATIONS

Table 1. General Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK25_REF Clock Output					
CLK25_REF Frequency		25		MHz	
V_{OH}		1.05		V	Load = 10 pF
V_{OL}		0		V	Load = 10 pF
CLK25_REF Duty Cycle	45		55	%	Load = 10 pF
LongTerm Jitter (RMS)			40	ps	

[1] Load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

[2] R_P and C_P are the values of the equivalent parallel RC circuit to ac ground ($R_P||C_P$), modeling the driving point impedance of the XTAL_I/CLK_IN pin.

Table 2. 10BASE-T1L Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltage Range					
AVDD_H	3.13	3.3	3.46	V	2.4 V p-p or 1.0 V p-p transmit level
AVDD_L	1.71	1.8 or 3.3	3.46	V	
AVDD_H, AVDD_L	1.71	1.8	3.46	V	1.0 V p-p transmit level
DVDD_1P1	1.0	1.1	1.2	V	
VDDIO	1.71	1.8, 2.5, or 3.3	3.46	V	
1.0 V p-p Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = DLDO_1P1
AVDD_x Supply Current, I_{AVDD}		25		mA	
Power Consumption		45		mW	100% data throughput, full activity
		11		mW	Software power-down mode
1.0 V p-p Transmit Level (Dual Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = external 1.1 V
AVDD_x Supply Current, I_{AVDD}		16		mA	
DVDD_1P1 Supply Current, I_{DVDD}		9		mA	
Power Consumption		39		mW	100% data throughput, full activity
2.4 V p-p Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 3.3 V, DVDD_1P1 = DLDO_1P1
Supply Current, I_{AVDD}		33		mA	
Power Consumption		109		mW	100% data throughput, full activity
		22		mW	Software power-down mode
2.4 V p-p Transmit Level (Dual Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = DLDO_1P1
AVDD_x Supply Current, I_{AVDD}		16.5		mA	
VDDIO Supply Current, I_{VDDIO}		15		mA	
Power Consumption		81		mW	100% data throughput, full activity
		11		mW	Software power-down mode
2.4 V p-p Transmit Level (Triple Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = external 1.1 V
AVDD_x Supply Current, I_{AVDD}		16.5		mA	
VDDIO Supply Current, I_{VDDIO}		6		mA	
DVDD_1P1 Supply Current, I_{DVDD}		9		mA	
Power Consumption		75		mW	100% data throughput, full activity
ANALOG INPUTS AND OUTPUTS					
MDI Gain Offset	−7.5		+3.5	%	
TIMING/LATENCY					
MII Latency					

SPECIFICATIONS

Table 2. 10BASE-T1L Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Transmit (TX) Latency		<1.8		µs	18-bit times
Receiver (RX) Latency		<3.2		µs	32-bit times
Total Latency		≤5		µs	

TIMING CHARACTERISTICS

POWER-UP TIMING

Table 3.

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t_1	Minimum time interval to internal power good[1]	20		43	ms
t_2	Hardware configuration latch time	6	8	14	µs
t_3	Management interface active			50	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

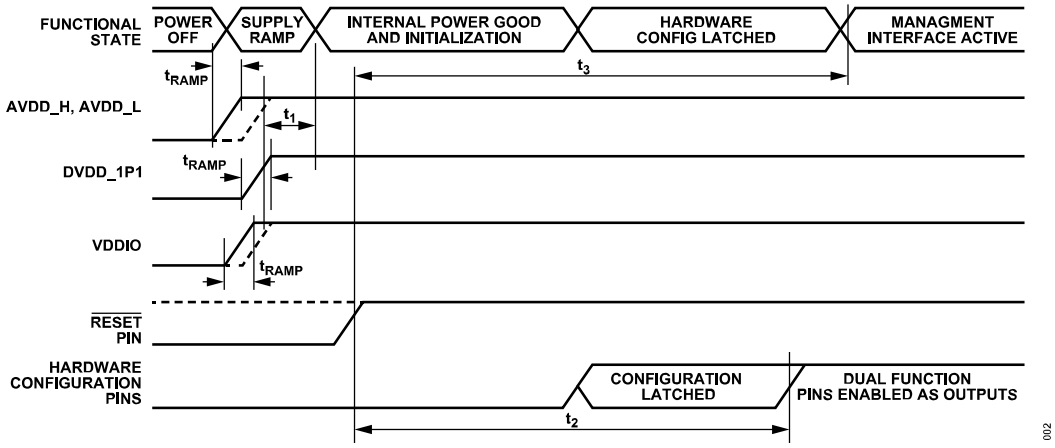


Figure 2. Power-Up Timing

MANAGEMENT INTERFACE TIMING

Table 4.

Parameter	Description	Min	Typ	Max	Unit
t_1	MDC period	400			ns
t_2	MDC high time	100			ns
t_3	MDC low time	100			ns
t_4	MDC rise or fall time			5	ns
t_5	MDIO signal setup time to MDC	10			ns
t_6	MDIO signal hold time to MDC	10			ns
t_7	MDIO delay time to MDC			300	ns

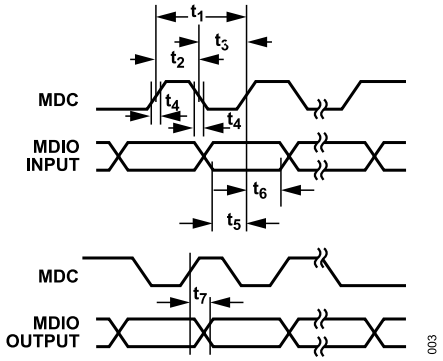


Figure 3. Management Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDDIO to GND	−0.3 V to +4 V
DVDD_1P1, DLDO_1P1 to GND	−0.3 V to +1.35 V
AVDD_H, AVDD_L to GND	−0.3 V to +4 V
MAC Interface[1], MDIO, MDC, $\overline{INT}$ to GND	−0.3 V to VDDIO + 0.3 V
TXN, TXP, RXN, RXP to GND	−0.3 V to AVDD + 0.3 V
LED_x, $\overline{RESET}$, LINK_ST/PHYAD_2 to GND	−0.3 V to VDDIO + 0.3 V
XTAL_I/CLK_IN to GND	−0.3 V to +2.75 V
XTAL_O, CLK25_REF to GND	−0.3 V to +1.35 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] See the Pin Configuration and Function Descriptions section for the full list of MAC interface pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
CP-40-29[2]	45	22	°C/W

[1] θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

[2] Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

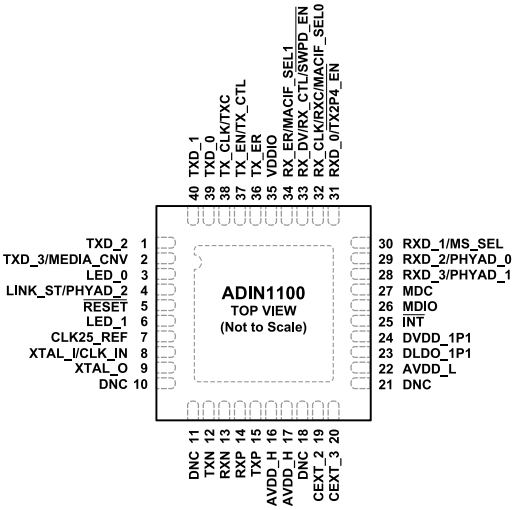
Table 7. ADIN1100, 40-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM		
TXN, TXP, RXN, RXP Pins	8000	3B
All Other Pins	2000	2
FICDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. THESE PINS MUST BE LEFT OPEN CIRCUIT.
2. EXPOSED PAD (GROUND). THIS GND PADDLE MUST BE CONNECTED TO GROUND. THE LFCSP PACKAGE HAS AN EXPOSED PAD THAT NEEDS TO BE CONNECTED TO GND FOR ELECTRICAL REASONS AND MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS. A 4 × 4 ARRAY OF THERMAL VIAS BENEATH THE EXPOSED GND PAD IS ALSO RECOMMENDED.

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic[1]	PU/PD[2]	Description
Clock Interface			
7	CLK25_REF	N/A	Analog Reference Clock Output. The 25 MHz reference clock from the crystal oscillator is available on the CLK25_REF pin. This pin can be used as an input to another PHY. The 25 MHz clock output is briefly disabled (logic low) following a software reset (25 ms) or a hardware reset (70 ms). See the Reset Operations section for more details.
8	XTAL_I/CLK_IN	N/A	Input for Crystal (XTAL_I). Single-Ended 25 MHz Reference Clock or 50 MHz Clock Input for RMII (CLK_IN).
9	XTAL_O	N/A	Crystal Output. If using a single-ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open circuit. See the External 25 MHz Clock Input for MII and RGMII Modes section.
Management Interface			
25	$\overline{\text{INT}}$	PU	Management Interface Interrupt Pin Output. Open-drain, active low output. A low on $\overline{\text{INT}}$ indicates an unmasked management interrupt. This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
26	MDIO	PU	Management Data Input/Output Synchronous to the MDC Clock. This pin is open-drain and requires a 1.5 kΩ pull-up resistor to VDDIO.
27	MDC	PD	Management Data Clock Input up to 2.5 MHz.
Reset			
5	$\overline{\text{RESET}}$	PU	Hardware Reset, Active Low Input. Hold low for >10 µs to reset the device. This pin can be left floating if a hardware reset is not required. See the Hardware Reset section.
Media Dependent Interface (MDI)			
12	TXN	N/A	Transmit Negative Pin.
13	RXN	N/A	Receive Negative Pin.
14	RXP	N/A	Receive Positive Pin.
15	TXP	N/A	Transmit Positive Pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic[1]	PU/PD[2]	Description
MAC Interface			
1	TXD_2	PD	Reduced Gigabit Media Independent Interface (RGMII)/MII Transmit Data 2 Input. See the MAC Interface section.
2	TXD_3/MEDIA_CNV	PD	RGMII/MII Transmit Data 3 Input (TXD_3). See the MAC Interface section.
			Media Converter Hardware Configuration Pin (MEDIA_CNV).
28	RXD_3/PHYAD_1	PD	RGMII/MII Receive Data 3 Output (RXD_3). See the MAC Interface section.
			PHY Address Hardware Configuration Pin 1 (PHYAD_1).
29	RXD_2/PHYAD_0	PD	RGMII/MII Receive Data 2 Output (RXD_2). See the MAC Interface section.
			PHY Address Hardware Configuration Pin 0 (PHYAD_0).
30	RXD_1/MS_SEL	PD	RGMII/RMII/MII Receive Data 1 Output (RXD_1). See the MAC Interface section.
			Leader/Follower Selection (MS_SEL). Set high for prefer leader selection and low for prefer follower selection. See Table 18.
31	RXD_0/$\overline{\text{TX2P4\_EN}}$	PD	RGMII/RMII/MII Receive Data 0 Output (RXD_0). See the MAC Interface section.
			Transmit Level Amplitude Hardware Configuration Pin ($\overline{\text{TX2P4\_EN}}$). Set high for 1 V p-p transmit amplitude. A low supports both 1 V p-p and 2.4 V p-p transmit amplitudes. See Table 19.
32	RX_CLK/RXC/MACIF_SEL0	PD	2.5 MHz MII Receive Clock Output (RX_CLK).
			2.5 MHz RGMII Receive Clock Output (RXC).
			MAC Interface Selection Hardware Configuration Pin 0 (MACIF_SEL0). See the MAC Interface Selection section.
33	RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$	PD	RMII/MII Mode Received Data Valid Output (RX_DV). This signal is known as CRS_DV in RMII mode. When asserted high, RX_DV indicates that valid data is present on the RXD_x lines.
		PD	RGMII Mode Receive Control Signal (RX_CTL). RX_CTL is a combination of the RX_DV and RX_ER signals using both edges of RXC.
			Software Power-Down Configuration ($\overline{\text{SWPD\_EN}}$). Set $\overline{\text{SWPD\_EN}}$ low to configure the PHY to enter software power-down mode after power-up or reset. See Table 17.
34	RX_ER/MACIF_SEL1	PD	RMII/MII Mode Receive Error Detected Output (RX_ER). When asserted high, RX_ER indicates that the PHY has detected a receive error.
			MAC Interface Selection Hardware Configuration Pin 1 (MACIF_SEL1). See Table 21.
36	TX_ER	PD	RMII/MII Mode Transmit Error Input Detection from the MAC to the PHY.
37	TX_EN/TX_CTL	PD	RMII/MII Mode Transmit Enable Input from the MAC to the PHY (TX_EN). TX_EN indicates that transmission data is available on the TXD_x lines.
			RGMII Mode Transmit Control Signal (TX_CTL). TX_CTL is a combination of the TX_EN and RX_ER signals using both edges of TXC.
38	TX_CLK/TXC	PD	2.5 MHz MII Transmit Clock Output (TX_CLK).
			2.5 MHz RGMII Transmit Clock Input (TXC).
39	TXD_0	PD	RGMII/RMII/MII Transmit Data 0 Input. See the MAC Interface section.
40	TXD_1	PD	RGMII/RMII/MII Transmit Data 1 Input. See the MAC Interface section.
Status			
3	LED_0	PU	General-Purpose, Programmable LED Indicator 0. The LED can be active high or active low. By default, LED_0 is configured to turn on when a link is established and blink when there is activity. See the Status LEDs section.
4	LINK_ST/PHYAD_2	PD	Link Status Output (LINK_ST). LINK_ST indicates whether a valid link has been established. LINK_ST is active high.
			PHY Address Hardware Configuration Pin 2 (PHYAD_2).
6	LED_1	PD	General-Purpose, Programmable LED Indicator 1. The LED can be active high or active low. By default, LED_1 is disabled. See the Status LEDs section.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic[1]	PU/PD[2]	Description
LDO and Reference Decoupling			
19	CEXT_2	N/A	External Decoupling for LDO Circuit. Connect a 0.1 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
20	CEXT_3	N/A	External Decoupling for LDO Circuit. Connect a 1 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
Power and Ground Pins			
16, 17	AVDD_H	N/A	Analog Supply Voltage for the Various Analog Circuits in the Device. This supply rail can be supplied by 1.8 V to 3.3 V depending on the transmit level configuration. If AVDD_H is 3.3 V, both 1.0 V p-p and 2.4 V p-p transmit operating modes are supported. If AVDD_H is 1.8 V, only 1.0 V p-p transmit operating mode is supported. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
22	AVDD_L	N/A	Analog Supply Voltage for the Internal LDO Circuits. This supply rail can be supplied by 1.8 V to 3.3 V. AVDD_L can be connected directly to the AVDD_H rail in long reach applications or alternatively to the VDDIO rail when the device is configured with dual supplies for lower power consumption. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
23	DLDO_1P1	N/A	Output from an Internal 1.1 V LDO Circuit. This pin can be connected to DVDD_1P1 to eliminate an additional power supply rail. Connect a 0.68 µF capacitor to ground as close as possible to this pin.
24	DVDD_1P1	N/A	Input for 1.1 V DVDD_1P1 Supply Rail. When using the internal LDO regulator, connect this pin directly to the DLDO_1P1 pin. Alternatively, an external 1.1 V rail can be provided to the DVDD_1P1 pin for greater power efficiency. Connect a 0.1 µF to ground as close as possible to this pin.
35	VDDIO	N/A	3.3 V, 2.5 V, or 1.8 V Digital Power for MDIO and MAC Interface. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to the pin.
41	EP (GND)	N/A	Exposed Pad (Ground). This GND paddle must be connected to ground. The LFCSP package has an exposed pad that needs to be connected to GND for electrical reasons and must be soldered to a metal plate on the PCB for mechanical reasons. A 4 × 4 array of thermal vias beneath the exposed GND pad is also recommended.
Other Pins			
10, 11, 18, 21	DNC	N/A	Do Not Connect. These pins must be left open circuit.

[1] Where a pin is shared between a functional signal and a hardware configuration pin signal, the hardware configuration pin signal is listed last.

[2] PU/PD refers to internal/on-chip pull-up or pull-down resistors. All of the hardware configuration pins have internal pull-down resistors. The default mode of operation without any external resistors connected to these pins is shown in Table 14. If an alternative mode of operation is required, use 4.7 kΩ pull-up resistors. N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

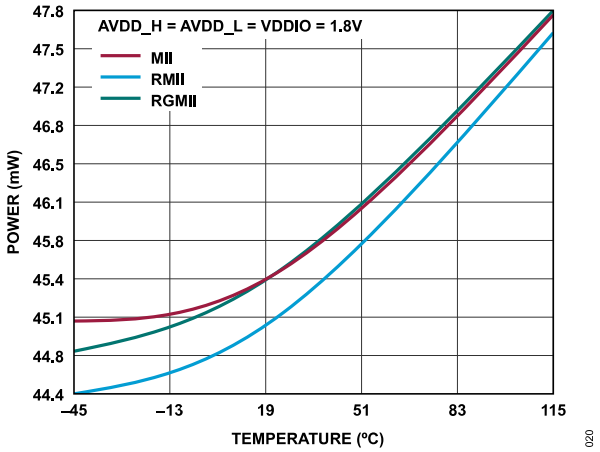


Figure 5. Power vs. Temperature, 1.8 V Single Supply, Internal LDO Circuit, 10BASE-T1L Mode

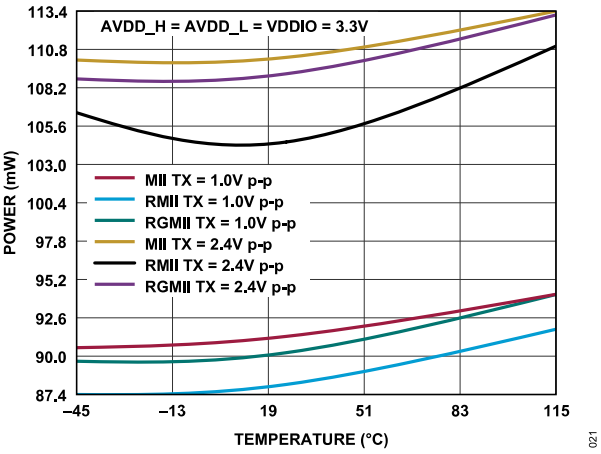


Figure 6. Power vs. Temperature, 3.3 V Single Supply, Internal LDO Circuit, 10BASE-T1L Mode

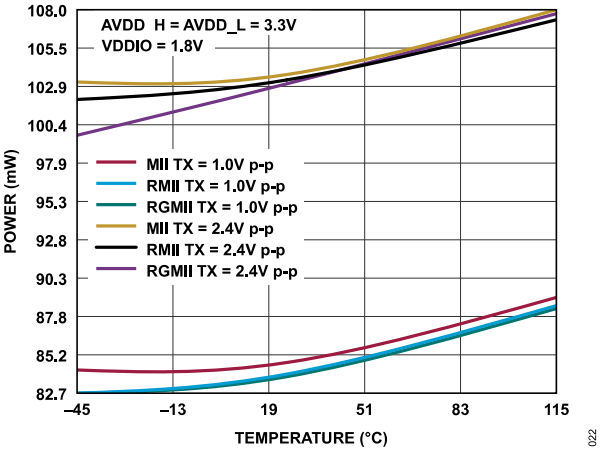


Figure 7. Power vs. Temperature, AVDD_H = 3.3 V, AVDD_L = 3.3 V, VDDIO = 1.8 V, Internal LDO Circuit, 10BASE-T1L Mode

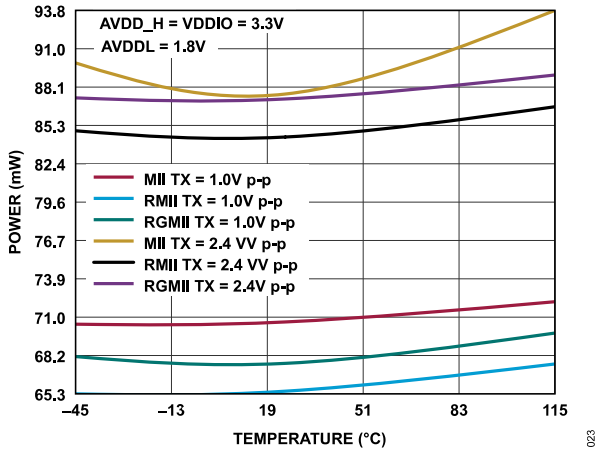


Figure 8. Power vs. Temperature, AVDD_H = 3.3 V, VDDIO = 3.3 V, AVDD_L = 1.8 V, Internal LDO Circuit, 10BASE-T1L Mode

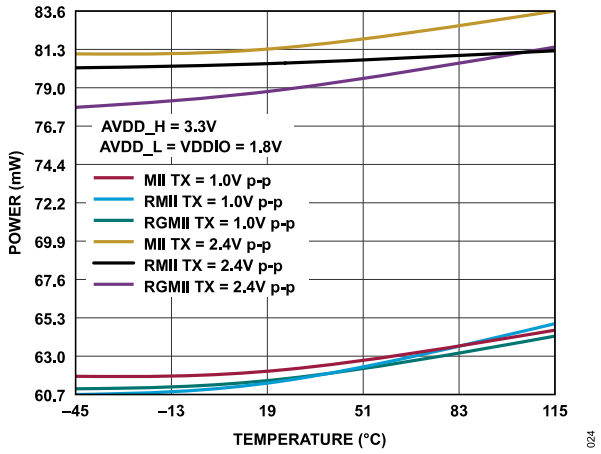


Figure 9. Power vs. Temperature, AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, Internal LDO Circuit, 10BASE-T1L Mode

THEORY OF OPERATION

The ADIN1100 is a low power, single port 10BASE-T1L Ethernet PHY device, compliant with the IEEE 802.3cg Ethernet standard for long reach, 10 Mbps single pair Ethernet.

The ADIN1100 integrates the following features:

- PHY core with common analog circuitry
- Input and output clock buffering
- MDIO interface to control subsystem registers, clock, and software resets
- MAC interface control logic
- Hardware configuration pins
- Configurable hardware interrupt pin
- Two configurable LED pins

POWER SUPPLY DOMAINS

The ADIN1100 has four power supply domains and requires a minimum of one supply rail.

- AVDD_H is the analog power supply input for the analog front end (AFE) circuitry in the ADIN1100.
- AVDD_L is the analog supply voltage for the internal LDO circuits. AVDD_L can be connected to the AVDD_H rail in single supply mode, or to an alternative lower voltage rail in dual supplies mode for lower power consumption.
- DVDD_1P1 is the 1.1 V digital core power supply input. It can operate from the internal 1.1 V LDO output available on the DLDO_1P1 pin. Alternatively, DVDD_1P1 can be driven from an external 1.1 V supply for lower power consumption.
- VDDIO is the digital power supply input for the ADIN1100 MAC interface, MDIO, and digital inputs/outputs (I/Os). It can be connected directly to the AVDD_L rail or to an external power rail.

The System Level Power Management section describes various application circuits that can be used as reference.

Single-Supply Applications

In a single-supply application, connect AVDD_H and AVDD_L to VDDIO, and in the ADIN1100, use the internal 1.1 V LDO circuit for DVDD_1P1. The appropriate supply voltage used depends on the end application and cable length. A recommended circuit is shown in the Single-Supply Configuration section.

Long Reach and Trunk/Spur Applications

The 1.0 V p-p transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. The ADIN1100 in this mode supports intrinsic safety applications.

The higher transmit operating mode of 2.4 V p-p supports trunk applications and requires a higher AVDD_H supply voltage of 3.3 V. This mode can be used for longer cable lengths in industrial Ethernet environments with higher noise levels.

MAC INTERFACE

The ADIN1100 provides the option of MII, RMII, or RGMII MAC interfaces. The MAC interface is selected using the hardware configuration pins (RX_CLK/RXC/MACIF_SEL0 and RX_ER/MACIF_SEL1) or via the management interface (MDIO). The two hardware configuration pins for MAC interface selection strap the ADIN1100 configuration after power-up, hardware reset, or software reset.

By default (hardware configuration pins floating), the MAC interface is configured in RMII mode. See the MAC Interface Selection for more details on how to configure the MAC interface using the hardware configuration pins.

It is recommended to use the hardware configuration pins for the MAC interface selection because the supported interfaces have different clock and pin mapping requirements.

MII Interface Mode

For the MII receive interface, the ADIN1100 generates a 2.5 MHz reference clock on RX_CLK to synchronize the RXD_3 to RXD_0 receive data signals. RX_DV indicates to the MAC that valid data is present on the RXD_3 to RXD_0 signals. RX_ER is driven high by the ADIN1100 if an error was detected in the frame that was received from the MDI interface and is being transmitted to the MAC interface.

For the MII transmit interface, the ADIN1100 generates a 2.5 MHz reference clock on TX_CLK. The MAC transmits data on TXD_3 to TXD_0 that is synchronized with TX_CLK. The MAC asserts TX_EN high to indicate to the ADIN1100 that transmission data is available on the TXD_3 to TXD_0 signal lines.

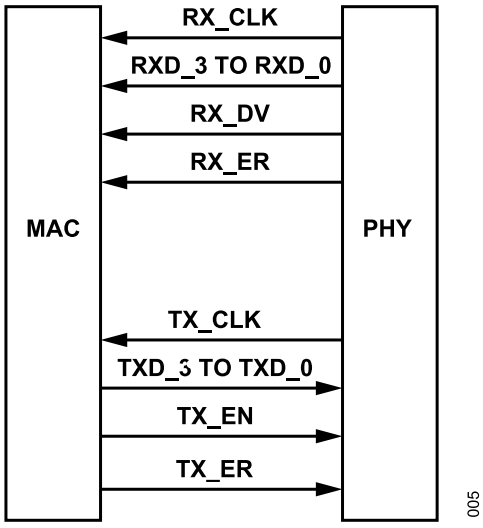


Figure 10. MII MAC PHY Interface Signals

THEORY OF OPERATION

RMII Interface Mode

RMII mode requires an external 50 MHz clock, which can be sourced externally from a MAC chip or a reference clock and applied to the ADIN1100 XTAL_I/CLK_IN pin. The 50 MHz clock is used for both the transmit and receive interfaces.

The receive data, RXD_1 to RXD_0, transitions synchronously to the reference clock (REF_CLK). The carrier sense and received data valid signal (CRS_DV) is a combination of the carrier sense and RX_DV signals, and is asserted while the receive medium is not idle. CRS_DV is asserted asynchronously to REF_CLK and deasserted synchronously.

RX_ER is also synchronous to the reference clock signal (REF_CLK) and asserted when an error is detected in the received frame or when a false carrier is detected. RX_ER assertion on a false carrier can be disabled by software.

Do not configure the MAC interface to RMII in software without ensuring the required 50 MHz clock is available. See MAC Interface Configuration Register for more details on RMII interface parameters.

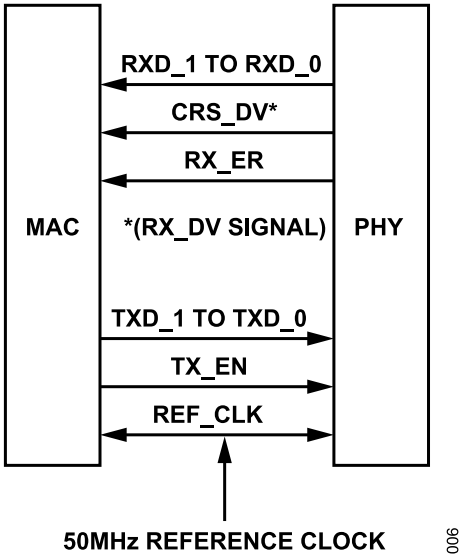


Figure 11. RMII MAC PHY Interface Signals

RGMII Interface Mode

For the RGMII receive interface, the ADIN1100 generates a 2.5 MHz RXC signal to synchronize RXD_3 to RXD_0. RX_CTL is a combination of the RX_DV and RX_ER signals (as described in Table 8) using both edges of the RXC signal. The ADIN1100 transmits the RX_DV signal on the positive edge of RXC and a combination (XOR function) of RX_DV and RX_ER on the negative edge of RXC.

For the RGMII transmit interface, the MAC generates a 2.5 MHz reference clock on TXC. The TXC clock is driven by the switch MAC. The MAC transmits the TXD_3 to TXD_0 data on both edges of TXC. TX_CTL is a combination of the TX_EN and TX_ER signals using both edges of TXC. TX_EN is transmitted on the positive edge of TXC, and a combination (XOR function) of TX_EN and TX_ER is transmitted on the negative edge of TXC.

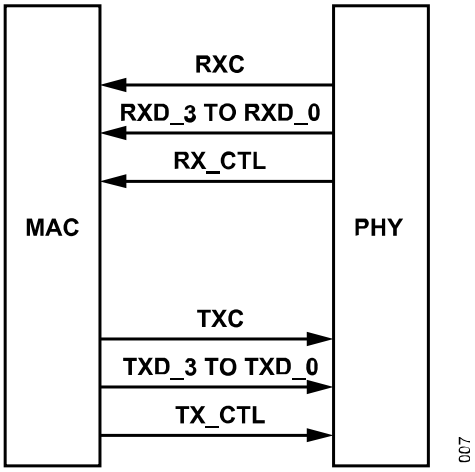


Figure 12. RGMII MAC PHY Interface Signals

TRANSMIT AMPLITUDE CONFIGURATION

The ADIN1100 supports two transmit amplitude modes of operation, as follows:

- 1.0 V p-p and 2.4 V p-p mode (high level)
- 1.0 V p-p only mode

The high level transmit operating mode allows the ADIN1100 to support both voltage levels. The operating level can then be automatically configured during autonegotiation (if enabled) based on the link partner capabilities. Note that the high level transmit operating mode of 2.4 V p-p requires an AVDD_H supply voltage of 3.3 V. Otherwise, if the supply voltage is less than 3.3 V, the device may not start up correctly.

The mode of operation is configured through the $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal (see the Transmit Amplitude section). The ADIN1100 also configures the default value for the transmit level register bits used for the autonegotiation process based on the level configured with the RX_D0/ $\overline{\text{TX2P4\_EN}}$ pin (see the Transmit Amplitude Advertisement section).

The ADIN1100 is configured in high level transmit operating mode by default if the RX_D0/$\overline{\text{TX2P4\_EN}}$ pin is left floating (internal pull-down resistor).

LEADER/FOLLOWER CONFIGURATION

The 10BASE-T1L standard uses a leader/follower clock scheme. This scheme is commonly used in full duplex transceiver standards with echo cancellation. One PHY is designated as the leader, and the other PHY as the follower. Autonegotiation is used to determine which PHY is the leader and which is the follower. leader and follower assignment does not generally matter.

THEORY OF OPERATION

Hardware Configuration

The ADIN1100 can be configured to prefer follower or prefer leader through the RXD_1/MS_SEL hardware configuration pin. The recommendation is to select prefer follower or prefer leader (see the Leader/Follower Preference section). If autonegotiation is disabled, the MS_SEL hardware configuration pin signal sets the default leader/follower selection. The ADIN1100 is configured in prefer follower by default if the pin is left floating (internal pull-down resistor).

Software Configuration

The leader and follower configuration bit (CFG_MST) is automatically updated after power-up, hardware reset, or software reset based on the MS_SEL hardware configuration pin signal level. This bit is only used when autonegotiation is disabled. Otherwise, this bit is set or reset during the autonegotiation process (see the Autonegotiation section).

AUTONEGOTIATION

The ADIN1100 uses the autonegotiation capability in accordance with IEEE 802.3 Clause 98, providing a mechanism for exchanging information between the local device and link partners to agree to a common mode of operation. Single twisted pair autonegotiation is performed using differential Manchester encoding (DME) pages exchanged between the local device and its link partner. At a high level, the autonegotiation provides the following functions:

- Transmit
- Receive
- Half duplex
- Arbitration

During the autonegotiation process, the local device advertises its own capabilities and compares them to those received from the link partner. The arbitration mechanism defines the operating mode selected so that the transmit amplitude mode and leader/follower selection are configured for the linked devices.

If the link is dropped, the autonegotiation process restarts automatically. An autonegotiation restart can also be requested by writing to the autonegotiation restart bit (AN_RESTART) in the autonegotiation control register (AN_CONTROL).

The autonegotiation process can take time to complete, depending on the number of pages exchanged, but is always the fastest way to bring up a link. Clause 98 of the IEEE 802.3 standard details the sequence timers and DME pages timing related to autonegotiation.

Autonegotiation is enabled by default for the ADIN1100, and it is strongly recommended to always keep it enabled.

Transmit Amplitude Advertisement

High Voltage Transmit Ability Advertisement

The B10L_TX_LVL_HI_ABLE bit configures the default values for the autonegotiation advertisement parameters. This bit is read only and configured based on the TX2P4_EN hardware configuration pin signal as described in the Transmit Amplitude section. The transmit amplitude advertisement parameters are defined with the following bits:

- AN_ADV_B10L_TX_LVL_HI_ABL: advertisement of the 10BASE-T1L high level transmit operating mode ability bit
- AN_ADV_B10L_TX_LVL_HI_REQ: advertisement of the 10BASE-T1L high level transmit operating mode request bit
- B10L_TX_LVL_HI: 10BASE-T1L transmit voltage amplitude control bit

Table 9. AN_ADV_B10L_TX_LVL_HI_ABL Settings

Bit Setting	Description
0	Support 1.0 V p-p transmit level only
1	Support both 1.0 V p-p and 2.4 V p-p transmit level

Table 10. AN_ADV_B10L_TX_LVL_HI_REQ Settings

Bit Setting	Description
0	Request 1.0 V p-p transmit level
1	Request 2.4 V p-p transmit level

High Voltage Transmit Level Request Advertisement

The ADIN1100 can be configured to advertise a request for the 2.4 V p-p transmit level using the 10BASE-T1L high level transmit operating mode ability advertisement bit (AN_ADV_B10L_TX_LVL_HI_ABL). Note that the 2.4 V p-p transmit level must be enabled using the $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal to enable the high voltage request advertisement.

Link Partner Transmit Level Advertisement

The high level transmit information advertised from the link partner can be read using the following bits:

- AN_LP_ADV_B10L_TX_LVL_HI_ABL: Link Partner 10BASE-T1L high level transmit operating mode ability
- AN_LP_ADV_B10L_TX_LVL_HI_REQ: Link Partner 10BASE-T1L high level transmit operating mode request

These bits are updated during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) is set.

THEORY OF OPERATION

Transmit Amplitude Resolution

Overview

Autonegotiation supports the following features to define the transmit amplitude to use between a local node and its link partner:

- Advertise the high voltage transmit ability from the local node
- Request to use the high voltage transmit level from the local node
- Read the link partner transmit level ability and transmit level request
- Autonegotiation and transmit level operating mode selection

If the ADIN1100 is configured in high voltage mode, the autonegotiation process determines the level to use based on the link partner capabilities.

Determination of Transmit Level Resolution

For a 10BASE-T1L link, if either the local or remote PHY advertises that it is not capable of supporting the high level (2.4 V p-p) transmit operating mode or if neither the local nor remote PHY advertises a request for high level (2.4 V p-p) transmit operating mode, the result is operation at the 1.0 V p-p transmit level.

If both the local and remote PHYs advertise that they are capable of transmitting in the high level (2.4 V p-p) transmit operating mode and if either the local or remote PHY advertises a request for high level (2.4 V p-p) transmit operating mode, the result is operation at the 2.4 V p-p transmit level.

Thus, a PHY can ensure that the device must operate at the 1.0 V p-p transmit level. But it can only request operation at the 2.4 V p-p transmit level.

Software Configuration

The ADIN1100 transmit level can also be configured in software using the following 10BASE-T1L autonegotiation advertisement bits:

- AN_ADV_B10L_TX_LVL_HI_ABL: high level transmit operating mode ability bit
- AN_ADV_B10L_TX_LVL_HI_REQ: high level transmit operating mode request register bits

The higher transmit level must be enabled with the $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal to configure the two autonegotiation advertisement bits through software. See the Transmit Amplitude section for details.

If it is required to only operate the PHY at 1.0 V p-p transmit level operation, clear the AN_ADV_B10L_TX_LVL_HI_ABL bit, so that 2.4 V p-p transmit level operation is not advertised. In this case, autonegotiation can only resolve to 1.0 V p-p transmit level operation, irrespective of the setting that the remote PHY advertises.

Table 11. Determination of Transmit Level by Autonegotiation

AN_LP_ADV_B10L_TX_LVL_HI_ABL	AN_LP_ADV_B10L_TX_LVL_HI_REQ	AN_ADV_B10L_TX_LVL_HI_ABL	AN_ADV_B10L_TX_LVL_HI_REQ	Transmit Level
0	X[1]	0	X[1]	1.0 V p-p
1	X[1]	0	X[1]	1.0 V p-p
0	X[1]	1	X[1]	1.0 V p-p
1	0	1	0	1.0 V p-p
1	0	1	1	2.4 V p-p
1	1	1	0	2.4 V p-p
1	1	1	1	2.4 V p-p

[1] X means don't care.

THEORY OF OPERATION

Leader/Follower Advertisement

On a 10BASE-T1L link, a local node and its remote link partner advertise their role capabilities whether they can operate as leader, follower, prefer leader, or prefer follower.

The ADIN1100 PHY provides the following functions:

- Leader/follower configuration advertisement
- Forced leader/follower configuration advertisement
- Read link partner leader/follower configuration

Leader/Follower Configuration Advertisement

The leader/follower configuration register bit (AN_ADV_MST) is used to configure the PHY to advertise its leader/follower configuration. Note that this bit is configured after power-up, hardware reset, or software reset based on the MS_SEL configuration pin signal status and can be overridden by software via the MDIO interface.

Forced Leader/Follower Configuration Advertisement

The ADIN1100 PHY can be forced to operate as a leader/follower. Forced configuration must be used with caution because a configuration fault can occur if the link partner is also set in forced mode as a leader/follower, resulting in autonegotiation failure. The ADIN1100 can be forced to operate as a leader or follower using the force leader/follower configuration bit (AN_ADV_FORCE_MS) in the BASE-T1 autonegotiation advertisement register, Bits[15:0] (AN_ADV_ABILITY_L).

Read Link Partner Leader/Follower Configuration

The link partner advertised leader/follower setting can be read using the following bits:

- AN_LP_ADV_FORCE_MS: link partner force leader/follower configuration register bit
- AN_LP_ADV_MST: link partner leader/follower configuration register bit

These bits are updated during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) is set.

Leader/Follower Resolution

Determination of Leader/Follower Configuration

On a 10BASE-T1L link, when the local and remote PHYs have the same preferred configuration, for example, both follower or both leader, autonegotiation randomly assigns compatible configurations to the local and remote PHYs. When one PHY has a forced configuration, its leader/follower configuration is given priority over a PHY with a preferred setting.

Leader/Follower Configuration Resolution

The ADIN1100 leader/follower configuration defined by the autonegotiation can be checked using the leader/follower resolution result register bits (AN_MS_CONFIG_RSLTN). The bits indicate if the PHY is configured as leader or follower or if there was a configuration fault.

These bits are updated during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) is set.

Table 12. Determination of Leader/Follower by Autonegotiation

Local[1]		Remote[1]		Local	Remote
AN_ADV_FORCE_MS	AN_ADV_MST	AN_LP_ADV_FORCE_MS	AN_LP_ADV_MST	Leader/Follower Resolution	
0	0	0	0	Leader/follower	Follower/leader
0	0	0	1	Follower	Leader
0	1	0	0	Leader	Follower
0	1	0	1	Leader/follower	Follower/leader
0	X	1	0	Leader	Follower
0	X	1	1	Follower	Leader
1	0	0	X	Follower	Leader
1	1	0	X	Leader	Follower
1	0	1	0	Configuration fault	Configuration fault
1	0	1	1	Follower	Leader
1	1	1	0	Leader	Follower
1	1	1	1	Configuration fault	Configuration fault

[1] X means don't care.

THEORY OF OPERATION

Autonegotiation Fail

On a 10BASE-T1L link, the autonegotiation can fail and can be caused by various scenarios.

- Configuration fault such as invalid leader/follower configuration
- Link quality issues
- Timeout in pages transmission

If the autonegotiation fails, the link remains down until the autonegotiation process is restarted and completed.

MANAGEMENT INTERFACE

The MII management interface provides a 2-wire serial interface between a host controller or external MAC chip and the ADIN1100 allowing access to control and status information in the subsystem and PHY core management registers.

The MII management interface consists of the following:

- MDC: clock line
- MDIO: bidirectional data line
- PHYAD_0, PHYAD_1, PHYAD_2: PHY address selection
- $\overline{\text{INT}}$: configurable management interrupt

The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures (see the MDIO Interface section).

MDI Circuitry

The MDI connects the ADIN1100 to the Ethernet network via a twisted wire pair.

The ADIN1100 requires an external hybrid circuit between the TXN/TXP and RXN/RXP pins and the 10BASE-T1L twisted wire pair. This function of the hybrid is to remove the local transmitted signal from the combined signal on the cable, thereby allowing full duplex operation on the 10BASE-T1L twisted wire pair.

The ADIN1100 hybrid requires a specific topology and values for proper operation. Figure 13 to Figure 15 show the topologies and values for the components. Consider the size, power, and voltage rating of these components in the context of other system requirements, for example, requirements for intrinsic safety.

The component values are as follows:

- R1 and R2 are termination resistors. The nominal value for both resistors is 50 Ω. Typically, 49.9 Ω may be chosen from the E96 series as per IEC 60063.
  - R1, R2: 49.9 Ω ± 1% tolerance
- R3 and R4: The nominal value is 5 kΩ ± 1% tolerance.
  - R3, R4: 4.99 kΩ ± 1% tolerance or 5.10 kΩ ± 1% tolerance are chosen from the E96 series.
- R5 and R6: The nominal value is 10 kΩ ± 1% tolerance.
  - R5, R6 = 10.0 kΩ when R3, R4 = 4.99 kΩ or 10.20 kΩ when R3, R4 = 5.1 kΩ.
  - R5 = R6 = 2 × R3 = 2 × R4.
- D1, D2: protection components low capacitance (<5 pF), low voltage (standoff voltage ≥3.3 V) TVS.
- C1, C2: 0.22 µF, 60 V rating. If transformer with low inductance is 350 µH, then C1 and C2 may need to increase to 0.47 µF (to comply with droop specification per IEEE 802.3).
- R7, R8: Optional resistors preventing built up charge on the capacitors C1 and C2 (100 kΩ to ~ 1 MΩ).
- C3, C4: 47 pF to 100 pF, ± 5% tolerance
- D3: protection component low capacitance TVS (≤ 100 pF). It is important that the TVS diode has low capacitance.
- L1 transformer: provides galvanic isolation.
  - Must be able to operate in the frequency range from 100 kHz to 20 MHz.
  - Inductance > 350 uH
- L2 common mode inductor: ≥220 µH, low leakage inductance <0.5 µH.
- L3 power inductor: power coupling for advanced physical layer (APL) devices and non APL devices.
  - APL: >880 µH differentially to achieve 10% max droop.
    - Recommended >220 µH coupled inductor (two inductors on a common magnetic core).
    - Or two > 440 µH individual inductors.
  - Non APL: >160 µH differentially to achieve approximately 25% max droop.
    - Recommended >47 µH coupled inductor (two inductors on a common magnetic core).
    - Or two >100 µH individual inductors.

    Note: If an isolation transformer is present on the MDI transmission line, the parallel combination between the transformer inductance and the total differential inductance of the power inductor must be greater than 160 µH.

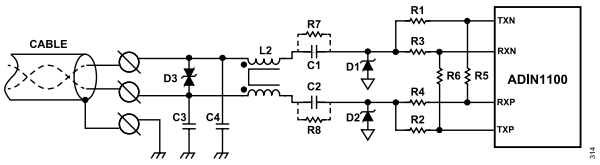


Figure 13. Recommended MDI Circuitry with Capacitive Coupling for the ADIN1100

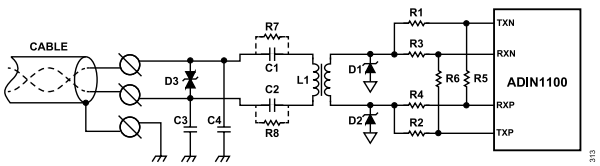


Figure 14. Recommended MDI Circuitry with Galvanic Isolation for the ADIN1100

THEORY OF OPERATION

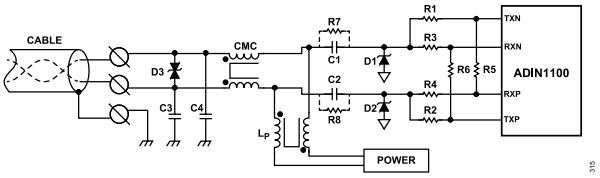


Figure 15. Recommended MDI Circuitry with Power Coupling for the ADIN1100

Hardware Interrupt ($\overline{INT}$)

The ADIN1100 can generate a hardware interrupt to a host controller or external MAC chip using the $\overline{INT}$ pin.

PHY Status Interrupts

The following conditions can be selected to generate an interrupt:

- MAC interface frame checker/generator interrupt
- MAC interface buffers overflow/underflow interrupt
- Autonegotiation status change interrupt
- Link status change interrupt

Those conditions can be set to enable an interrupt on the $\overline{INT}$ pin using PHY_SUBSYS_IRQ_MASK (see the PHY Subsystem Interrupt Mask Register section).

Following a hardware interrupt on the $\overline{INT}$ pin, the interrupt source can be checked using PHY_SUBSYS_IRQ_STATUS (see the PHY Subsystem Interrupt Status Register section).

Hardware Reset Interrupt

The ADIN1100 can also be configured to generate a hardware interrupt after a hardware reset ($\overline{RESET}$ pin pulled low) by setting the enable hardware reset interrupt bit (CRSM_HRD_RST_IRQ_EN) in CRSM_IRQ_MASK (see the System Interrupt Mask Register section).

Following a hardware interrupt on the $\overline{INT}$ pin, the interrupt source can be checked with the CRSM_HRD_RST_IRQ_LH bit in CRSM_IRQ_STATUS (see the System Interrupt Status Register section).

Software Requested Interrupt

For system validation with an external host controller, the ADIN1100 can be requested to generate a hardware interrupt on the $\overline{INT}$ pin using the CRSM_SW_IRQ_REQ bit in CRSM_IRQ_MASK (see the System Interrupt Mask Register section).

Following a hardware interrupt on the $\overline{INT}$ pin, the interrupt source can be checked with the CRSM_SW_IRQ_LH bit in CRSM_IRQ_STATUS (see the System Interrupt Status Register section).

System Error Interrupts

The ADIN1100 can also generate system errors interrupts. The interrupt flags are located within the reserved bit sections of CRSM_IRQ_STATUS (see the System Interrupt Status Register section).

CRSM_IRQ_MASK (see the System Interrupt Mask Register section) must be configured to allow system error interrupts. Refer to Table 98 for details on the interrupts mask. The ADIN1100 must be hardware reset to recover from a system error interrupt (CRSM_IRQ_STATUS reserved bits read as 1).

RESET OPERATIONS

Overview

The ADIN1100 supports the following chip resets:

- Power-on reset
- Hardware reset
- Software reset
- MAC interface reset
- PHY subsystem reset

All of these resets put the ADIN1100, including the PHY core, into a known state. Whenever the PHY core is reset, the ADIN1100 MAC interface output pins are driven to a low state.

Power-On Reset

The ADIN1100 includes a power supply monitoring circuit to ensure that the chip has the correct voltage supply before initiating the power-up sequence. During power-up, the ADIN1100 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good.

Hardware Reset

A hardware reset is initiated by the power-on reset circuitry or by asserting the $\overline{RESET}$ pin low for a minimum of 10 µs. The ADIN1100 includes a deglitch circuitry on this pin to reject pulses shorter than 1 µs.

When the $\overline{RESET}$ pin is deasserted, all the input/output (I/O) pins are held in tristate mode, the hardware configuration pins are latched, and the I/O pins are configured to their functional mode. When all the external and internal supplies are valid and stable, the crystal oscillator circuit is enabled. After the crystal has started up and stabilized, the phase-locked loop (PLL) is enabled. After a delay of 50 ms (maximum) from the deassertion of the $\overline{RESET}$ pin, all the internal clocks are valid, the internal logic is released from reset, and all the management interface registers are accessible over the MDIO interface.

THEORY OF OPERATION

The CLK25_REF clock output stays low while the $\overline{\text{RESET}}$ pin is asserted low and remains low for another 70 ms (maximum) after the $\overline{\text{RESET}}$ pin is deasserted.

Software Reset

A full chip software reset is initiated by setting the software reset bit (CRSM_SFT_RST). When this bit is set, the chip fully initializes, almost equivalent to a hardware reset except that it does not go through the voltage supply validation sequence. The I/O pins are held in tristate mode, the hardware configuration pins are latched, and then the I/O pins are configured to their functional mode. The crystal oscillator circuit is enabled, and after the crystal has started up and stabilized, the PLL is enabled. Approximately 10 ms (maximum) after setting the CRSM_SFT_RST bit, the internal logic is released from reset and all the management interface registers are accessible. The system ready bit (CRSM_SYS_RDY) indicates that the start-up sequence is complete and the system is ready for normal operation.

The CLK25_REF clock output remains low for 25 ms (maximum) following a software reset.

PHY Subsystem Reset

A PHY subsystem reset is initiated on the ADIN1100 by setting the PHY subsystem reset register bit (CRSM_PHY_SUBSYS_RST) to 1. The reset is applied for typically 1.2 µs, and then this bit self clears. All of the PHY digital circuitry is reset, and any available active link drops. The PHY subsystem reset does not alter the values of the management registers, which remain accessible throughout the sequence. The subsystem reset is a short reset and can be used to put the device into a known state while retaining the internal register contents.

MAC Interface Reset

A MAC interface reset is initiated on the ADIN1100 by setting the PHY MAC interface reset register bit (CRSM_MAC_IF_RST) to 1. The reset is applied for typically 1.2 µs, and then this bit self clears. A reset sequence is provided to the ADIN1100 MAC interface, but without dropping the available active link. This reset interrupts any packet transmission or reception on the MAC interface, but does not drop an existing active link nor prevent a link from being established. The MAC interface reset does not alter the values of the management registers, which remain accessible throughout the sequence.

STATUS LEDS

Overview

The LED_0 and LED_1 is only available in ADIN1100 pins can be used to connect external LEDs to indicate the ADIN1100 link status and transmit or receive activity. The activity assigned to each LED is configurable through LED_CNTRL (see the LED Control Register section).

The LED pins are suitable for ultra low power LEDs. The maximum output current for the LED_0 and LED_1 pins is 8 mA with a VDDIO = 3.3 V. For higher LED power requirements, the use of an external transistor is recommended, as described in the Transistor Controlled LED section.

The LED_x pins can also be connected to a host microcontroller GPIO (configured as a pulse-width modulated input or hardware interrupt). This configuration can be useful in applications where the user interface must be fully handled by an external host controller (for example, an external LED module or display).

If the LED_0 and LED_1 pins are directly connected to a host controller, it is recommended to place a low value resistance in series between the ADIN1100 LED_x pins and the host controller to avoid any potential current surge. The resistor value must be defined based on host controller capabilities and the ADIN1100 LED_x pin output current capabilities listed in Table 1.

LED Pin Multiplexing

For the LED_1 pin only, an internal multiplexer must be configured to enable the LED_1 signal on the pin. LED_1 is disabled by default and can be enabled using the DIGIO_LED1_PINMUX bits (see the Pin Mux Configuration 1 Register section).

The LED_0 pin does not need multiplexing.

LED Polarity

The LED_0 and LED_1 pins can be configured to support various LED circuit polarities through the LED polarity mode feature (see the LED Polarity Register section). Three polarity modes are available for each LED, as follows:

- Autosense (default)
- Active high
- Active low

In autosense mode, the ADIN1100 automatically senses the pin at power-up or reset to select the appropriate polarity configuration.

In active high mode, the ADIN1100 is configured to drive the LED from the anode side.

In active low mode, the ADIN1100 is configured to drive the LED from the cathode side.

Example circuits are described in the LED Circuit Examples section.

LED Function

LED_0 and LED_1 can be configured to display various activities of the ADIN1100 using the LED function feature. The LED function

THEORY OF OPERATION

is configurable using the LED0_FUNCTION and LED1_FUNCTION bits (see the LED Control Register section).

Note that the 7, 8, 9, and 10 (decimal) bit settings for LEDx_FUNCTION are not available in LED Mode 2.

LED Mode

LED_0 and LED_1 activity behavior can be configured using the two LED modes, as follows:

- LED Mode 1: blink duty cycle defined using the LED0_BLINK_TIME_CNTRL (see the LED_0 On/Off Blink Time Register section)
- LED Mode 2: blink duty cycle automatically defined by the ADIN1100 based on activity level (%)

LED_x Pins Configuration Summary

See Table 13 for the configuration options of the LED_x pins.

Table 13. LED_x Pins Configuration Summary

Parameter	LED_0	LED_1
Pin Number	3	6 (ADIN1100 only)
Internal Pull-Up or Pull-Down Resistor	Pull-up	Pull-down
Status at Power-Up or Reset	Enabled	Disabled (via pin mux)
LED Pin Mux	Not applicable	DIGIO_LED1_PINMUX bits (see the Pin Mux Configuration 1 Register section)
Enable LED	LED0_EN bit (see the LED Control Register section)	LED1_EN bit (see the LED Control Register section)
LED Polarity	LED0_POLARITY bits (see the LED Polarity Register section)	LED1_POLARITY bits (see the LED Polarity Register section)
LED Mode	LED0_MODE bit (see the LED Control Register section), default: LED Mode 1	LED1_MODE bit (see the LED Control Register section), default: LED Mode 1
LED Function[1]	LED0_FUNCTION bits (see the LED Control Register section), default: LINKUP_TXRX_ACTIVITY	LED1_FUNCTION bits (see the LED Control Register), default: TXRX_ACTIVITY
LED Blink Rate	LED0_BLINK_TIME_CNTRL (see the LED_0 On/Off Blink Time Register section)	LED1_BLINK_TIME_CNTRL (see the LED_1 On/Off Blink Time Register section)
Maximum Current[2]	8 mA at 3.3 V	8 mA at 3.3 V

[1] The 7, 8, 9, and 10 (decimal) settings in the LEDx_FUNCTION bits are not available in Mode 2.

[2] See Table 1 for details.

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LINK STATUS PIN

Overview

The link status pin (LINK_ST/PHYAD_2) is asserted high when the link status bit (AN_LINK_STATUS) is asserted and indicates that the link between the ADIN1100 and its link partner is active.

The LINK_ST/PHYAD_2 pin has a weak internal pull-down resistor. The pin is also used as a hardware configuration pin signal (PHYAD_2) during power-up, hardware reset, or software reset.

Typical Use

The link status pin can be used to connect an external LED or can be connected to a host microcontroller GPIO (configured as a pulse-width modulated input or hardware interrupt).

By default, the LINK_ST signal is active high and can be configured as either active high or low using the link status polarity bit (DGIO_LINK_ST_POLARITY). See the Pin Mux Configuration 1 Register section.

The link status pin is not intended to source current. Use the circuit recommendation in the Transistor Controlled LED section as a reference to interface an LED on this pin. If the link status pin is directly connected to a host controller, it is recommended to place a low value resistance in series between the ADIN1100 link status pin and the host controller to avoid any potential current surge. The resistor value must be defined based on host controller capabilities.

POWER-DOWN MODES

The ADIN1100 supports two power-down modes.

- Hardware power-down
- Software power-down

Hardware Power-Down Mode

The hardware power-down mode can be used when no operation is required on the ADIN1100 and the power consumption needs to be minimized.

The device enters hardware power-down mode when the $\overline{\text{RESET}}$ pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the clocks are gated off, and all the I/O pins are held in tristate mode.

In this mode, the ADIN1100 power consumption is equivalent to the internal circuit leakage. The internal registers are not accessible in this mode.

Software Power-Down Mode

The software power-down mode can be used to configure the ADIN1100 registers before bringing a link up. In this mode, the analog and digital circuits are in a low power state, and the PLL is active and can provide output clocks if configured to do so. Any signals exposed to the MDI pins (TXP, TXN, RXP, RXN) are ignored and any active link is dropped. The MAC interface output pins are asserted low and internal registers are accessible using the MDIO interface.

The device can be configured to automatically enter software power-down mode after power-up, hardware reset, or software reset using the $\overline{\text{SWPD\_EN}}$ hardware configuration pin signal. The ADIN1100 can also be instructed to enter software power-down mode by setting the software power-down bit (CRSM_SFT_PD).

The software power-down status bit (CRSM_SFT_PD_RDY) indicates that the device is in software power-down mode.

The ADIN1100 exits software power-down mode when the CRSM_SFT_PD bit is cleared. After exiting software power-down and if autonegotiation is completed, the device attempts to bring a link up.

HARDWARE CONFIGURATION PINS

OVERVIEW

The ADIN1100 can operate in unmanaged or managed configurations with the use of the hardware configuration pins.

The hardware configuration pins are standard pins with an alternate bootstrap function. The ADIN1100 reads the configuration pin level immediately after power-up, hardware reset, or software reset, and configures the PHY settings accordingly. When active, the ADIN1100 immediately attempts to bring up a link and the hardware configuration pins can then be used with their main pin function. These pins can be used in unmanaged or managed configuration.

The unmanaged configuration refers to the ADIN1100 operating in standalone mode. This mode can be used when the system requires a static configuration of the ADIN1100 without the need for software control and an external host controller.

The managed configuration refers to the use of an external host such as a microcontroller to control and manage the ADIN1100 by software over the MDIO interface. The configuration pins can be connected to the external host or hardware configured using pull-up/pull-down resistors. When active, the host controller can override any of the ADIN1100 hardware configurations set by the hardware pins after power-up, hardware reset, or software reset.

UNMANAGED APPLICATIONS

In unmanaged applications, it is possible to configure the desired operation of the ADIN1100 using hardware configuration pins without any software intervention. The hardware configuration pins set the default values of the corresponding management registers after power-up, hardware reset, or software reset.

Software power-down after reset must be disabled for unmanaged applications or the ADIN1100 remains in power-down indefinitely because the device can only exit power-down from register operation using the management interface (see the Software Power-Down Mode section).

MANAGED APPLICATIONS

In managed applications, the ADIN1100 can be configured by a host controller via the management interface. The host controller can dynamically configure the device as required by the application.

In managed applications, the software power-down after reset functionality can be enabled as the host controller brings the ADIN1100 to active mode using the management interface.

HARDWARE CONFIGURATION PINS FUNCTIONS

Overview

The following functions are configurable from the ADIN1100 hardware configuration pins:

- PHY address
- Software power-down mode after reset
- Transmit amplitude configuration
- Leader/follower selection
- MAC interface selection (RGMII/RMII/MII)
- Media converter operation

All of the hardware configuration pins have internal pull-down resistors. The default mode of operation is shown in Table 14. If an alternative mode of operation is required, refer to Table 15 for the suggested external pin control.

Table 14. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode (Pin Floating)
PHY Address	0x0
Software Power-Down Mode After Reset	Enabled
Leader/Follower Selection	Prefer follower
Transmit Amplitude	1.0 V p-p and 2.4 V p-p
MAC Interface Selection	RMII
Media Converter	Normal PHY operation

Table 15. Recommended Control for Hardware Configuration Pins

Required Pin Level	Managed Configuration Options	Unmanaged Configuration Options
High	4.7 kΩ external pull-up resistor Host GPIO output high[1]	4.7 kΩ external pull-up resistor
Low	External pull-down resistor Host GPIO output low[1] Host GPIO tristated[2] Floating pin[2]	External pull-down resistor Floating pin[2]

[1] A low value series resistor is recommended.

[2] External pull-down resistor is recommended.

Media Converter

The ADIN1100 can operate as a media converter, which allows a 10BASE-T PHY to be connected directly to the ADIN1100 via the RMII or RGMII. The ADIN1100 can connect to a 10BASE-T1L remote PHY via the MDI pins.

In RMII mode, the MEDIA_CNV hardware configuration strap pin can be used to enable the media converter functionality by default after reset or power cycle. Alternatively, the media converter can be configured via the CRSM_RMII_MEDIA_CNV_EN bits (see the MAC Interface Configuration Register section).

In RGMII mode, the ADIN1100 can be directly connected to another RGMII device without any media configuration requirements.

The MEDIA_CNV hardware configuration pin signal is shared with TXD_3, which is not used in RGMII mode (see the MAC Interface section). The TXD_3/MEDIA_CNV pin has a weak internal pull-down resistor. Thus, by default, the ADIN1100 is configured for normal PHY operation (for example, external MAC chip connected on the MAC interface). An external pull-up resistor or external host

HARDWARE CONFIGURATION PINS

control via a GPIO must be used to select the media converter operation in RMII mode.

Table 16. Media Converter Selection (Hardware Configuration)

MEDIA_CNV	Media Converter Selection
0	Normal PHY operation
1	Media converter operation

PHY Address Configuration

The ADIN1100 PHY address can be configured using three pins:

- RXD_2/PHYAD_0
- RXD_3/PHYAD_1
- LINK_ST/PHYAD_2

These are two-level configuration pins, which means that it is possible to configure the ADIN1100 to any of the eight available PHY addresses. The PHY address pins have weak internal pull-down resistors. Thus, by default, the ADIN1100 is configured with PHY Address 0x0.

Particular attention is required if these three pins are used in managed applications and connected to an external host controller because the PHY address is set after power-up, hardware reset, or software reset.

Software Power-Down After Reset

The $\overline{\text{SWPD\_EN}}$ hardware configuration pin signal is shared with the RX_DV signal and is used to enable or disable the software power-down after reset feature. The power-down bit (CRSM_SFT_PD) is set based on the $\overline{\text{SWPD\_EN}}$ signal status during power-up, hardware reset, or software reset. CRSM_SFT_PD can also be set using the MDIO interface to enable software power-down after reset.

The RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$ pin has a weak internal pull-down resistor. Thus, by default, the ADIN1100 is configured with software power-down after reset enabled.

When software power-down after reset is enabled, the ADIN1100 enters software power-down after power-up, hardware reset, or software reset. Software power-down provides a lower power mode where most of the ADIN1100 internal modules are turned off.

The ADIN1100 can be configured to exit power-down by setting the CRSM_SFT_PD bit to 0 using the MDIO interface.

Following a power-up, hardware reset, or software reset, and if autonegotiation is enabled and software power-down after reset is disabled, the ADIN1100 starts autonegotiation and tries to bring up a link.

Table 17. Software Power-Down (Hardware Configuration)

$\overline{\text{SWPD\_EN}}$	Software Power-Down Configuration
0	PHY in software power-down after reset
1	PHY not in software power-down after reset

Leader/Follower Preference

The MS_SEL hardware configuration pin signal is shared with the RXD_1 signal and configures the default leader/follower selection. If MS_SEL is pulled low during power-up, hardware reset, or software reset, the device is configured by default to prefer follower. If MS_SEL is pulled high during power-up, hardware reset, or software reset, the device is configured by default to prefer leader.

The RXD_1/MS_SEL pin has a weak internal pull-down resistor. Thus, by default, the ADIN1100 is configured to prefer follower.

The MS_SEL hardware configuration pin signal configures the default setting of the autonegotiation leader/follower configuration register bit (AN_ADV_MST). MS_SEL also configures the default setting of the leader/follower configuration register bit (CFG_MST), which is used when autonegotiation is disabled.

The AN_ADV_MST and CFG_MST bits can be modified using the MDIO interface but return to their default values set by the MS_SEL hardware configuration pin signal after power-up, hardware reset, or software reset.

Table 18. Leader/Follower Selection (Hardware Configuration)

MS_SEL	Leader/Follower Selection
0	Prefer follower selection
1	Prefer leader selection

Transmit Amplitude

The $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal is shared with the RXD_0 signal and is used to configure the default transmit amplitude mode. The transmit amplitude mode is defined by the pin status during power-up, hardware reset, or software reset as defined in Table 19.

The $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal configures the default setting of the high voltage transmit ability bit (B10L_TX_LVL_HI_ABLE).

The RXD_0/$\overline{\text{TX2P4\_EN}}$ pin has a weak internal pull-down resistor. Thus, by default, the ADIN1100 is configured to support both 1.0 V p-p and 2.4 V p-p voltage levels.

If the RXD_0/$\overline{\text{TX2P4\_EN}}$ pin is strapped high (1.0 V p-p only), the associated register cannot be changed through the MDIO interface. That is, 2.4 V p-p operation is not possible if the ADIN1100 has been hardware pin configured only for 1.0 V p-p.

HARDWARE CONFIGURATION PINS

Table 19. Transmit Amplitude Selection (Hardware Configuration)

$\overline{\text{TX2P4\_EN}}$	Transmit Amplitude Selection
0	1.0 V p-p and 2.4 V p-p
1	1.0 V p-p

If $\overline{\text{TX2P4\_EN}}$ is pulled low during power-up, hardware reset, or software reset, the 2.4 V p-p transmit operating mode is enabled and the value of B10L_TX_LVL_HI_ABLE is set to 1.

If $\overline{\text{TX2P4\_EN}}$ is pulled high during power-up, hardware reset, or software reset, the 2.4 V p-p transmit operating mode is disabled, and the value of B10L_TX_LVL_HI_ABLE is set to 0.

The B10L_TX_LVL_HI_ABLE bit reports whether the PHY is capable of operating in the 10BASE-T1L high transmit voltage mode, as described in Table 20.

Table 20. B10L_TX_LVL_HI_ABLE Settings

Bit Setting	Description
0	PHY does not support 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.
1	PHY supports 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.

MAC Interface Selection

The MAC interface hardware configuration pin signals (MACIF_SELx) are shared with the RX_CLK/RXC and RX_ER signals and can be configured according to Table 21. The RX_CLK/RXC/MACIF_SEL0 and RX_ER/MACIF_SEL1 pins have weak internal pull-down resistors. Thus, by default, the ADIN1100 is configured in RMII mode. External pull-up/pull-down resistors or host control via a GPIO must be used to select the RGMII or MII MAC interface mode.

Table 21. MAC Interface Selection (Hardware Configuration)

MACIF_SEL1	MACIF_SEL0	MAC Interface Selection
0	0	RMII
0	1	RGMII
1	0	Reserved
1	1	MII

BRINGING UP 10BASE-T1L LINKS

The following sections provide some recommendations on how to bring a link up between the ADIN1100 and a remote link partner. The sections cover various configurations and some may not be relevant to the intended application. Refer to the Theory of Operation section for more detailed explanations.

UNMANAGED PHY OPERATION

For an unmanaged PHY where there is no control of the ADIN1100 over the management interface, the hardware configuration pins determine the operating mode. See the Hardware Configuration Pins section for more details on how to use the hardware configuration pins. The following sections describe the steps required to bring up a link in unmanaged applications.

Set the PHY Address

The PHY address can be selected by asserting the PHY address pins: RXD_2/PHYAD_0, RXD_3/PHYAD_1, and LINK_ST/PHYAD_2.

When it exits reset, the ADIN1100 starts autonegotiation and tries to bring up a link after autonegotiation completes.

See the PHY Address Configuration section for details on how to use the address pins.

Disable Software Power-Down Mode After Reset

The software power-down mode must be disabled in unmanaged applications. Otherwise, the ADIN1100 remains in software power-down indefinitely. Assert the RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$ pin high during power-up and reset so that the PHY does not enter software power-down mode when it exits reset.

See the Software Power-Down After Reset section for details on how to configure the software power-down after reset function.

Leader/Follower Selection

The RXD_1/MS_SEL pin is used to configure the PHY to advertise prefer follower or prefer leader.

See the Leader/Follower Preference section for details on how to configure the leader/follower setting.

Set Transmit Amplitude Level

The RXD_0/$\overline{\text{TX2P4\_EN}}$ pin configures the PHY to advertise the support of both 1.0 V p-p and 2.4 V p-p transmit level operation or to only advertise support of 1.0 V p-p transmit level operation.

By default, the ADIN1100 is configured to support 1.0 V p-p and 2.4 V p-p transmit levels due to the internal pull-down resistor. Assert the relevant pin high or low to disable the support for the 2.4 V p-p transmit level.

See the Transmit Amplitude section for details on how to configure the transmit amplitude level.

Select the MAC Interface (RGMII/RMII/MII)

The MAC interface type can be selected using the RX_CLK/RXC/MACIF_SEL0 and RX_ER/MACIF_SEL1 pins.

See the MAC Interface Selection for details on how to select the MAC interface.

Enable the Media Converter Functionality

Assert the TXD_3/MEDIA_CNV pin high if media converter function is required (RMII mode only).

See the Media Converter section for details on how to enable the media converter functionality.

MANAGED PHY OPERATION

In a managed PHY application, a host controller such as a microcontroller is used to configure the ADIN1100 operation in software via the management interface (MDIO).

Similar to the unmanaged PHY operation, the hardware configuration pins can be used to set up the controlled ADIN1100 (see the Unmanaged PHY Operation section for details). Alternatively, the hardware configuration pins can directly be controlled by the host (for example, GPIO) via an external pull-up or pull-down resistor or both.

In managed applications, the software power-down after reset can be enabled. The ADIN1100 stays in software power-down mode until the software has configured the PHY to be active. When active, the PHY can then start autonegotiation and try to bring up a link.

Power-Up and Reset Complete

A typical way for software to verify that the device has completed the power-up and reset sequence and is available for normal operation is to read the management register that has the IEEE organizationally unique identifier (OUI), model, and revision numbers. The value of this register is unique to each PHY vendor and is a nonzero value. If the device has not completed the power-up, the value does not read correctly. In legacy BASE-T PHYs, this value is at management interface Register Address 0x2 and Register Address 0x3.

In the ADIN1100, the OUI, model number, and revision numbers can also be read at Device Address 0x1F Clause 45 only), Register Address 0x2, and Register Address 0x3 (Clause 22 and Clause 45).

MMD1_DEV_ID1 contains the OUI, Bits[3:18] (see the Vendor Specific 1 MMD Identifier High Register section).

BRINGING UP 10BASE-T1L LINKS

MMD1_DEV_ID2 contains the OUI, Bits[19:24] (MMD1_DEV_ID2_OUI), the model number (MMD1_MODEL_NUM), and the revision number (MMD1_REV_NUM). See the Vendor Specific 1 MMD Identifier Low Register section.

Table 22. ADIN1100 Unique Identifier Values

Description	Bit Name	Value
Organizationally Unique Identifier, Bits[3:18]	MMD1_DEV_ID1	0x283
Organizationally Unique Identifier, Bits[19:24]	MMD1_DEV_ID2_OUI	0x2F
Model Number, Bits[6:0]	MMD1_MODEL_NUM	0x8
Revision Number, Bits[6:0]	MMD1_REV_NUM	0x1

When a valid read of the IEEE OUI is done, the system ready bit (CRSM_SYS_RDY) can also be read to verify that the start-up sequence is complete and the system is ready for normal operation.

The software power-down status bit (CRSM_SFT_PD_RDY) can be read to check if the device is in the software power-down state. This bit is also controlled by the $\overline{\text{SWPD\_EN}}$ hardware configuration pin signal.

Configuring the Device for Linking

After power-up or reset, configure the ADIN1100 for the desired operation for linking. The ADIN1100 may already be configured as required by the hardware configuration pins, but greater control is available using the management registers.

The autonegotiation process is used to match the operating mode between a local and remote PHY. For example, autonegotiation is used to ensure that the modes agree between the two devices on which PHY operates as leader and which as follower. Autonegotiation is also used to match the transmit level between the two PHYs.

Autonegotiation is enabled by default for the ADIN1100, and it is strongly recommended to always keep Autonegotiation enabled. Autonegotiation is defined by the IEEE standard and includes a number of mechanisms to ensure robust linking operation between PHYs and is the fastest way to bring up a link.

Configuration of Transmit Level Mode

Overview

The ADIN1100 can support transmit level operation at either 1.0 V p-p or 2.4 V p-p if the B10L_TX_LVL_HI_ABLE bit is set to 1 and a 3.3 V supply is provided on the AVDD_H pins. The higher transmit level can support longer reach but also has higher power consumption.

The ADIN1100 can support 1.0 V p-p transmit level operation with a 1.8 V supply on the AVDD_H pins at very low power consumption.

The ADIN1100 can either be configured to advertise support of both 1.0 V p-p and 2.4 V p-p transmit level operation or to advertise support of only 1.0 V p-p transmit level operation. Refer to the Transmit Level Mode Advertisement section for more details.

1.0 V p-p transmit level operation is required for intrinsically safe operation.

Enable High Voltage Transmit Ability

The high voltage transmit ability is set using the $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal, which internally sets the high voltage transmit ability bit, B10L_TX_LVL_HI_ABLE (read only), as described in the Transmit Amplitude section.

Enable 1.0 V p-p and 2.4 V p-p Transmit Levels

To allow both 1.0 V p-p and 2.4 V p-p transmit level operation, set AN_ADV_B10L_TX_LVL_HI_ABL to 1 to indicate that the device is capable of 2.4 V p-p transmit level operation (a 3.3 V supply is required on the AVDD_H pins).

Set 2.4 V p-p Transmit Level as Preferred

If 2.4 V p-p transmit level operation is preferred, set AN_ADV_B10L_TX_LVL_HI_REQ to 1 to request 2.4 V p-p transmit level operation. Note that autonegotiation determines the transmit level that the link operates at.

Set 1.0 V p-p Transmit Level as Preferred

If 1.0 V p-p transmit level operation is preferred, set AN_ADV_B10L_TX_LVL_HI_REQ to 0. Autonegotiation determines the transmit level that the link operates at.

Enable 1.0 V p-p Transmit Level Only

If it is required to only operate the PHY at 1.0 V p-p transmit level operation, set AN_ADV_B10L_TX_LVL_HI_ABL to 0 so that 2.4 V p-p transmit level operation is not advertised.

In this case, autonegotiation can only resolve to 1.0 V p-p transmit level operation, irrespective of the setting that the remote PHY advertises. For very long cable lengths, depending on the characteristics of the cable, it may not be possible to bring up a link at 1.0 V p-p operation.

When the high level transmit is disabled through the RXD_D0/$\overline{\text{TX2P4\_EN}}$ pin, the AVDD_H supply can be supplied from either 1.8 V or 3.3 V for 1.0 V p-p transmit level operation.

Transmit Level Mode Advertisement

Enable High Voltage Transmit Ability

The AVDD_H power rail must be provided with a 3.3 V supply for the ADIN1100 to support the 2.4 V p-p transmit level.

The high voltage transmit ability is enabled on the ADIN1100 by setting the $\overline{\text{TX2P4\_EN}}$ hardware configuration pin signal low during power-up, hardware reset, or software reset. The transmit ability

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bit, B10L_TX_LVL_HI_ABLE (read only), is set automatically to the defined hardware configuration as follows:

- B10L_TX_LVL_HI_ABLE = 0: 1.0 V p-p only ability
- B10L_TX_LVL_HI_ABLE = 1: 1.0 V p-p and 2.4 V p-p ability

See the Configuration of Transmit Level Mode section for more details.

Advertise High Voltage Transmit Ability

Set the AN_ADV_B10L_TX_LVL_HI_ABL bit to 1 to advertise the high level transmit mode to the link partner during autonegotiation. This bit can only be set if the ADIN1100 has the ability to transmit in high voltage mode (B10L_TX_LVL_HI_ABLE = 1).

High voltage transmit ability only enables the ADIN1100 to advertise support for both 2.4 V p-p and 1.0 V p-p levels. The selected level is determined by autonegotiation with the link partner.

See the Transmit Amplitude Advertisement section for more details.

Advertise a Request for High Voltage Transmit Level

Set the AN_ADV_B10L_TX_LVL_HI_REQ bit to 1 to advertise a request for 2.4 V p-p transmit level operation during autonegotiation. This bit can only be set if the ADIN1100 has the ability to transmit in high voltage mode (B10L_TX_LVL_HI_ABLE = 1).

See the Transmit Amplitude Advertisement section for more details.

Read Link Partner Advertised Transmit Level

The link partner advertised transmit information can be read using the link partner high level transmit operating mode ability bit (AN_LP_ADV_B10L_TX_LVL_HI_ABL) and the link partner high level transmit operating mode request bit (AN_LP_ADV_B10L_TX_LVL_HI_REQ). These bits are valid when the autonegotiation is completed (AN_COMPLETE = 1).

See the Transmit Amplitude Advertisement section for more details.

Completion of Autonegotiation

When autonegotiation has completed, the autonegotiation complete indication register bit (AN_LINK_GOOD) is set. This bit indicates the completion of the autonegotiation sequence and that the enabled PHY link is setting up or active.

When autonegotiation has completed and the link is up, the autonegotiation complete register bit (AN_COMPLETE) is set to 1 and the contents of the following registers are valid:

- BASE-T1 autonegotiation advertisement registers
  - AN_ADV_ABILITY_L: Bits[15:0]
  - AN_ADV_ABILITY_M: Bits[31:16]
  - AN_ADV_ABILITY_H: Bits[47:32]
- BASE-T1 autonegotiation link partner base page ability registers
  - AN_LP_ADV_ABILITY_L: Bits[15:0]
  - AN_LP_ADV_ABILITY_M: Bits[31:16]
  - AN_LP_ADV_ABILITY_H: Bits[47:32]

Link Status

The status of the link can be determined by reading the link status register bit (AN_LINK_STATUS). This bit latches low.

When read as 1, this bit indicates that a valid link has been established.

If this bit reads 0, it means that the link has failed since the last time it was read. This bit latches low. Thus, if a 0 is read, this bit must be read a second time to determine if the link status has come up in the interim (see the Latch Low Registers section).

If the link is dropped, the autonegotiation process restarts automatically. Autonegotiation can be restarted by request through a write to the autonegotiation restart bit (AN_RESTART) in the AN_CONTROL register (see the BASE-T1 Autonegotiation Control Register section).

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LOOPBACK MODES

The PHY core provides the following loopback modes:

- Physical medium attachment (PMA) loopback
- Physical coding sublayer (PCS) loopback
- MAC interface loopback
- MAC interface remote loopback

These loopback modes test and verify various functional blocks within the PHY. The use of a frame generator and frame checkers allows completely self contained in-circuit testing of the digital and analog data paths within the PHY core.

PMA Loopback

In PMA loopback, the MDI interface must be left open circuit, thereby transmitting into an unterminated connector or cable. In this mode, the signal transmitted from the ADIN1100 is echoed back from the open 10BASE-T1L MDI. This test mode is an implementation of the PMA local loopback function defined in Subclause 146.5.6 of the IEEE Standard 802.3cg. Remove any cable connected to the MDI interface to improve the test mode accuracy.

In PMA loopback mode, the device must be configured in forced link configuration mode (autonegotiation disabled). To enable PMA loopback, set the 10BASE-T1L PMA loopback enable bit (B10L_LB_PMA_LOC_EN) to 1 (see the 10BASE-T1L PMA Control Register section).

PCS Loopback

PCS loopback mode loops the transmit data back to the receiver within the PCS block at the input stage of the PHY digital block. Setting the B10L_LB_PCS_EN bit (B10L_PCS_CNTRL register) enables PCS loopback.

When the PCS loopback mode is enabled, no signal is transmitted to the MDI pins.

MAC Interface Loopback

MAC interface loopback mode loops the data received on the MAC interface transmit data pins (TXD_x signals) back to the receive data pins (RXD_x signals) and can therefore be used to verify MAC interface connectivity. Set the MAC_IF_LB_EN bit to 1 (see the MAC Interface Loopbacks Configuration Register section) to enable MAC interface loopback.

If the MAC_IF_LB_TX_SUP_EN bit within the same register is set (enabled by default), the transmission of the signal received on the MAC interface is not transferred to the ADIN1100 PHY core.

MAC Interface Remote Loopback

MAC interface remote loopback requires a link up with a remote PHY and enables looping of the data received on the ADIN1100 to the remote PHY. This linking allows a remote PHY to verify a complete link by ensuring that the PHY receives the proper data. Set the MAC_IF_REM_LB_EN bit to 1 (see the MAC Interface Loopbacks Configuration Register) to enable MAC interface remote loopback.

If the MAC_IF_REM_LB_RX_SUP_EN bit (see the MAC Interface Loopbacks Configuration Register section) is set (set by default), the data received by the ADIN1100 from the MDI pins is not transferred through the MAC interface.

External MII/RMII Loopback

Overview

When configured in external MII/RMII loopback mode, the ADIN1100 echoes back the data received from a remote PHY. The external MII/RMII loopback is performed by physically connecting the MAC transmission signal pins to the MAC reception signal pins. The wiring configuration required is described in Table 23.

Table 23. External MII/RMII Loopback Wiring

Reception Signals	Transmission Signals
RXD_0	TXD_0
RXD_1	TXD_1
RXD_2[1]/PHYAD_0	TXD_2[1]
RXD_3[1]	TXD_3[1]
RX_DV[2]/CRS_DV[3]	TX_EN
RX_ER	TX_ER

[1] MII only.

[2] MII reference name.

[3] RMII reference name.

Software Configuration

For the external RMII loopback, the RMII TXD check enable bit, RMII_TXD_CHK_EN (see the RMII Configuration Register section), must be set to 1 so that CRS_DV can be connected to TX_EN.

The external MII loopback does not require any particular register bits to be set to be enabled.

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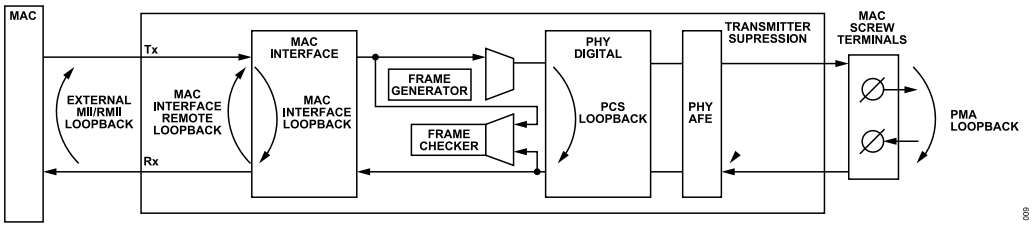

Figure 16. ADIN1100 Loopback Modes

FRAME GENERATOR AND CHECKER

Overview

The ADIN1100 can be configured to generate frames and to check received frames (see Figure 17). The generating and checking functions can be used together or independently. If the ADIN1100 transmitted frames are looped back at the remote end, the frame checker can be used to check the echoed self generated frames.

Frame Generator

When the frame generator is enabled, the MAC interface is ignored and the frame generator data is used for transmission on the MDI pins. To use the frame generator, the diagnostic clock must also be enabled using the CRSM_DIAG_CLK_EN bit (see the CRSM Diagnostics Clock Control Register section).

The frame generator control registers configure the type of frames to be sent (for example, random data, all 1s), the frame length, and the number of frames to be generated.

The generation of the requested frames starts by enabling the frame generator by setting the FG_EN bit (see the Frame Generator Enable Register section).

When the generation of the frames is completed, the frame generator done bit, FG_DONE, is set (see the Frame Generator Done Register section).

Frame Checker

The frame checker is enabled by setting the frame checker enable bit, FC_EN (see the Frame Checker Enable Register section). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY using the frame checker transmit select bit, FC_TX_SEL (see theFrame Checker Transmit Select Register section). The frame checker reports the number of frames received, cyclic redundancy check (CRC) errors, and various frame errors. The frame checker frame counter registers and the frame checker error counter registers count these events.

Error Counters

The frame checker counts the number of CRC errors, and these errors are reported in the receive error counter register (RX_ERR_CNT). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched copy of the receive frame counter register is available in FC_FRM_CNT_H (see the Frame Checker Count High Register section) and FC_FRM_CNT_L (see the Frame Checker Count Low Register section).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frames errors, and undersized frame errors.

The frame checker also counts frames with an odd number of nibbles in the frame, and counts packets with an odd number of nibbles in the preamble.

The frame checker also counts the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (SSD) state is entered.

FRAME GENERATOR AND CHECKER LINK TEST

Using the ADIN1100 and a second PHY device, the user can configure a convenient, self contained validation setup of the PHY to PHY connection. Figure 17 shows an overview of how each PHY is configured. An external cable is connected between both devices, and PHY 1 is generating frames using the frame generator. PHY 2 has MAC interface remote loopback enabled using MAC_IF_REM_LB_EN (see the MAC Interface Loopbacks Configuration Register section).

1. The PHY 1 frames (frame generator) are sent over the 10BASE-T1L single pair cable.
2. PHY 2 receives frames on the PHY 2 MDI pins.
3. The PHY 2 MAC interface loops the frame back.
4. The PHY 2 frames (looped back) are sent over the 10BASE-T1L single pair cable.
5. PHY 1 receives the PHY 2 frames (looped back) on the MDI pins.
6. The PHY 1 frame checker checks the received frames.

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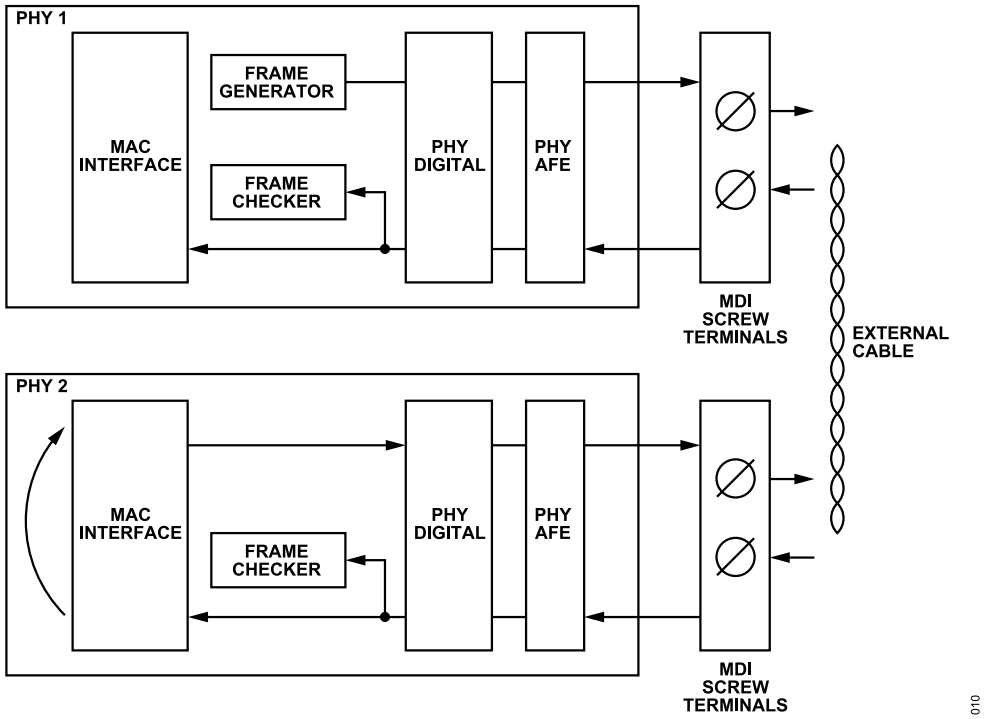

Figure 17. Remote Loopback Used Across Two PHYs for Self Check Purposes

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TEST MODES

The ADIN1100 provides several test modes as described in Subclause 146.5.2 from the IEEE 802.3cg™-2019 standard that allows testing of the transmitter waveform, distortion, jitter, and droop. These test modes change only the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from the normal operation.

Additionally, the ADIN1100 supports the transmit disable mode as described in Subclause 45.2.1.186a.2.

Table 24. ADIN1100 Test Modes Summary

Test Mode	Description
PMA Test Modes (Subclause 146.5.2)	
Test Mode 1	Transmitter output voltage and timing jitter test mode. When this mode is selected, the ADIN1100 repeatedly transmits the data symbol sequence (+1, –1).
Test Mode 2	Transmitter output droop test mode. In this mode, the ADIN1100 transmits ten +1 symbols followed by ten −1 symbols. This sequence is repeated indefinitely.
Test Mode 3	Normal operation in idle mode test mode. In this mode, the ADIN1100 transmits as in non test operation and in the leader data mode with the data set to normal interframe idle signals.
Transmit Disable Mode (Subclause 45.2.1.186a.2)	Both transmit and receive paths act like in normal operation mode but only transmit 0 symbols. This mode can be used to measure the MDI return loss specified in Subclause 146.8.3.

Enable the PMA Test Mode 1 to Test Mode 3

The ADIN1100 can be configured in one of the PMA test modes (Test Mode 1 to Test Mode 3) using the following procedure:

1. Enter software power-down mode by writing a 1 to the CRSM_SFT_PD bit in the CRSM_SFT_PD_CNTRL register (see the Software Power-Down Control Register section).
2. Check that the ADIN1100 has entered the software power-down mode by reading the CRSM_SFT_PD_RDY bit in the CRSM_STAT register (see the System Status Register).
3. Disable autonegotiation by writing a 0 to the AN_EN bit in the AN_CONTROL register (see the BASE-T1 Autonegotiation Control Register section).
4. Set autonegotiation forced mode by writing a 1 to the AN_FRC_MODE_EN bit in the AN_FRC_MODE_EN register (see the Autonegotiation Forced Mode Enable Register).
5. Select the desired test mode by writing the appropriate value to the B10L_TX_TEST_MODE bits in the B10L_TEST_MODE_CNTRL register (see the 10BASE-T1L Test Mode Control Register section). Table 25 outlines the bit settings for each PMA test mode.
6. Exit software power-down mode by writing 0 to the CRSM_SFT_PD bit in the CRSM_SFT_PD_CNTRL register (see the Software Power-Down Control Register section).

Table 25. PMA Test Modes Configuration

PMA Test Mode	B10L_TX_TEST_MODE, Bits[15:13] (Binary)
Test Mode 1	001
Test Mode 2	010
Test Mode 3	011

Enable Transmit Disable Mode

System Status RegisterThe ADIN1100 can be configured in transmit disable mode using the following procedure:

1. Enter software power-down mode by writing a 1 to the CRSM_SFT_PD bit in the CRSM_SFT_PD_CNTRL register (see the Software Power-Down Control Register section).
2. Check that the ADIN1100 has entered the software power-down mode by reading the CRSM_SFT_PD_RDY bit in the CRSM_STAT register (see the System Status Register section).
3. Disable autonegotiation by writing a 0 to the AN_EN bit in the AN_CONTROL register (see the BASE-T1 Autonegotiation Control Register section).
4. Set autonegotiation forced mode by writing a 1 to the AN_FRC_MODE_EN bit in the AN_FRC_MODE_EN register (see the Autonegotiation Forced Mode Enable Register section).
5. Set the transmit disable mode by writing a 1 to the B10L_TX_DIS_MODE_EN bit in the B10L_PMA_CNTRL register (see the 10BASE-T1L PMA Control Register section).
6. Exit software power-down mode by writing 0 to the CRSM_SFT_PD bit in the CRSM_SFT_PD_CNTRL register (see the Software Power-Down Control Register section).

TIME DOMAIN REFLECTOMETRY (TDR)

Given that the 10BASE-T1L compliant PHY enables communication over long cables, debugging a faulty cable can become costly and difficult without the right tools. To help with this, Analog Devices 10BASE-T1L products provide a TDR engine that enables cable fault detection, distance to fault, and cable length estimation.

The diagnostics solution is the combination of a highly accurate on-chip TDR engine and a set of algorithms that run on a host microcontroller, allowing maximum flexibility for a wide variety of cables and more advanced cable diagnostic capabilities.

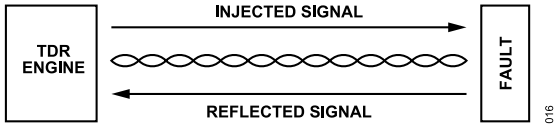

Figure 18. ADIN1100 TDR Engine

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Fault Detection with the TDR Engine

The Analog Devices algorithm has a time resolution of 8.3 ns, which translates to a length resolution of less than 1 m and a maximum of 1600 m, with an accuracy of 2%.

This fault detector algorithm is capable of finding open and short fault conditions even when the ADIN1100 is physically connected to another PHY through their MDI, which implies that the link partner PHY is potentially transmitting DME pages. Traditional TDR methods struggle to find faults if other signal sources or noise is also present in the same link. This is not the case of the Analog Devices solution, which makes it suitable for debugging when there is no control over the remote end.

The fault detector algorithm is provided as a C-code library containing the high-level functions required for diagnostics. These functions have been optimized to not utilize any advanced processing so that they can be executed by any low-power microcontroller.

A single function call is sufficient to execute the fault detector. The function returns the type of fault and the distance to the fault in meters from the MDI connector.

The fault detect TDR library can be requested from the software section in the landing page of the ADIN1100, ADIN1110, and ADIN2111.

TDR Offset Calibration

The library includes a function to calibrate the offset of the TDR measurement. This particular function in the library is useful given that different MDI circuits may introduce variable delays in the signal path, which can contribute to the offset of the length measurement. For instance, an isolation transformer on the MDI is highly likely to introduce a signal delay that corresponds to a couple of meters in length.

This calibration is not required to run the fault detector, and an average value is provided by default. However, it is recommended for short cables if accuracy is required. If this calibration is required, it can be done once in the lab for a specific MDI circuit implementation, and the offset value can then be stored in nonvolatile memory for future use.

To perform this calibration, the MDI port must be left open or shorted. No load or cable can be connected to the MDI port.

Cable Calibration

By default, the algorithm is optimized to support long reach cables compliant with the IEEE 802.3cg standard. However, given the wide variety of cable types, which have different insertion loss, return loss, and signal delay characteristics, the library includes a calibration function that optimizes the algorithm to operate with any cable, and estimates its nominal velocity of propagation (NVP) for more accurate length estimations. The length accuracy mainly depends on the accuracy of the NVP value.

To run this calibration, a cable with a known length must be attached to the MDI port, and its end must be left open or shorted. NVP values are generally between 0.5 and 0.9 and are a property of the construction of the cable. In general, an average NVP value of approximately 0.65 can be assumed. This calibration is not required to run the fault detector, unless higher length accuracy is needed or if nonstandard cables are utilized. This calibration can be done once in the laboratory for a given cable, and the values can be stored in nonvolatile memory.

Refer to the C-code driver for more information related to the usage of these functions.

Length/Distance to Fault Accuracy

The accuracy of the distance to a fault, or length measurements, mainly depends on the NVP value, which is determined by the accuracy of the cable length used to perform the NVP calibration.

Table 26 provides results for induced faults and distance-to-fault measurements for different cables and lengths. In all cases, the algorithm was successful finding the open or short conditions induced during the test. The NVP value for the Profibus PA cable used in this test was roughly estimated, and the same was used for the Cat5E and Cat6 cables.

Table 26. Length Estimation Error for Different Cables

Cable Type	Estimated Length (m)	Length Error (%)	Note
Fieldbus Type A - AWG 18	50.2	0.7	NVP calibrated
Fieldbus Type A - AWG 18	102.1	2.1	NVP calibrated
Fieldbus Type A - AWG 18	403.4	0.8	NVP calibrated
Fieldbus Type A - AWG 18	807.6	0.8	NVP calibrated
Fieldbus Type A - AWG 18	1045.3	1.0	NVP calibrated
Fieldbus Type A - AWG 18	1462.9	2.0	NVP calibrated
Cat5E	133.1	2.4	NVP not calibrated
Cat5E	244.4	1.8	NVP not calibrated
Cat6	73.6	5.1	NVP not calibrated
Cat6	137.2	5.6	NVP not calibrated

LINK QUALITY MONITORING

The ADIN1100, ADIN1101, ADIN1110, ADIN1111, and ADIN2111 provide the mean squared error (MSE) measurement of the received signal, which directly relates to the signal-to-noise ratio (SNR) seen by the PHY receiver. The MSE or SNR can be mapped to a signal quality indicator (SQI) and can be used for assessing the overall 10BASE-T1L link segment/channel quality.

The link quality may be affected by the cable length, the cable properties such as insertion and return loss, presence, quality and connection of the cable shield, number and quality of possible interconnections between cable segments, as well as level of noise in the environment around the devices and the cable. Therefore, the link quality can provide useful information during a device

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design, product testing, as well as at installation in the system, and during the lifetime of the system.

Signal-to-Noise Ratio and Bit Error Rate

There is a statistical relation between a communication channel SNR and bit error rate (BER). The relation between white noise SNR and 10BASE-T1L BER is shown in Figure 19.

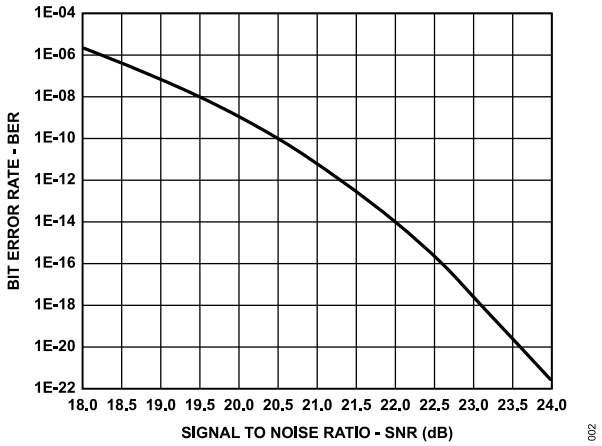

Figure 19. Statistical Relation Between SNR and BER in 10BASE-T1L

The IEEE 802.3cg-2019 standard requires the 10BASE-T1L BER ≤ 10^{-9}, in the presence of the relevant noise. For context, the BER 10^{-9} means 1 bit error every 100 sec in continuous 10 Mbps data, which translates to approximately an SNR of 20.0 dB on the 10BASE-T1L PHY as shown in Figure 19.

With an SNR of 21.0 dB, the BER must be 10^{-11}, which is 1 bit error every 10,000 sec or 2¾ hour, and with an SNR of 22.0 dB, the BER must be 10^{-14}, which is 1 bit error in 115 days. These examples illustrate how the SNR relates to the reliability of the 10BASE-T1L Ethernet.

There are always some errors in any data communication channel. The communication protocols, implemented and operating above the Ethernet physical layer, such as TCP/IP in general use cases, or the specific protocols for industrial or building automation ensure data integrity by frame repetition or error correction as appropriate for a given application. However, the link quality and related error rate of the physical layer must be kept at a certain level for reliable connection. The acceptable error rate may be different in noncritical monitoring compared to a time critical automation network or safety application.

Mean Squared Error at PHY Slicer

The link quality monitoring inside the PHY is implemented as an MSE measurement.

The 10BASE-T1L Ethernet uses PAM3 modulation—the data sent over the cable is coded into symbols of three voltage levels. Inside the receiver, after analog and digital signal processing, is a device called a slicer, which makes the decisions whether the incoming signal voltage level represents a +1, 0, or –1 symbol. An ideal received and scaled signal is already at these exact levels. However, the noise coupled to the Ethernet channel from various sources affects the real signal.

The PHY measures, for each received symbol, an error between the output of the slicer and the received signal already scaled to the correct amplitude level as shown in Figure 20. The mean square value of these errors is then calculated and reported in the PHY MSE_VAL register.

There is a direct relation between the MSE and SNR.

$$SNR = \frac{1}{MSE} \quad (1)$$

$$SNR(\text{dB}) = -MSE(\text{dB}) \quad (2)$$

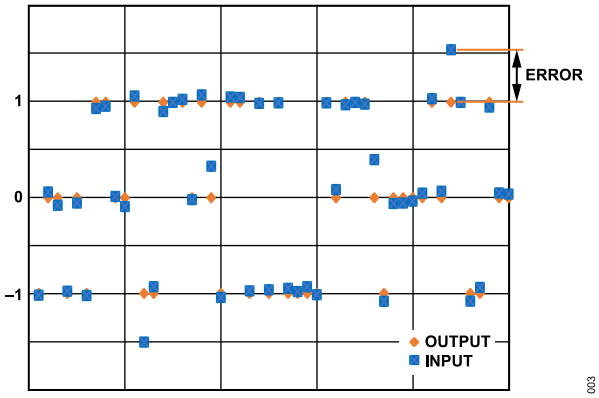

Figure 20. Error Between Ethernet PHY Slicer Input and Output

MSE Reading

The ADIN1100, ADIN1101, ADIN1110, ADIN1111, and ADIN2111 automatically measure the MSE in the background when the 10BASE-T1L link is active and makes it available in the MSE_VAL register.

The MSE_VAL register can be read via the management interface (MDIO or SPI) anytime. After power-up or reset, before the first link is up, the MSE_VAL register value is zero. When the 10BASE-T1L link is up, the MSE_VAL register is updated after each received symbol (every 133 ns). When the link drops, the register still updates. However, the MSE value is incorrect. Therefore, reading and processing the MSE is logical only when the 10BASE-T1L link is up.

The frequency of reading the MSE_VAL register is not limited, and it can be read as often as the management interface allows. Therefore, how often MSE_VAL must be read depends on how fast the link quality is expected to be changing and on how often the link quality needs to be assessed and reported or recorded in the end system application.

An example of polling the link status and reading the MSE is as follows:

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1. Read the PMA_PMD_STAT1 register (Device Address 0x01, Register Address 0x0001).
2. Check the PMA_LINK_STAT_OK bit (Bit 2, Mask 0x0004) value. If the bit value is 0, indicating the link is down, skip the following steps and start over again. If the bit value is 1, indicating link is up, continue with the following steps.
3. Read the MSE_VAL register (Device Address 0x01, Register Address 0x830B).
4. Process/use the measured MSE.

MSE Interpretation

The easiest use of the measured MSE is to compare the value read from the MSE_VAL register directly with the MSE register value range and to interpret the link quality as outlined in Table 27 or Table 28.

Alternatively, the MSE_VAL register value can be interpreted as the MSE as follows:

$$MSE\left(\text{dB}\right) = 10\log_{10}\left(MSE_{VAL} \times \frac{1.5523}{2^{18}}\right) \quad (3)$$

And the SNR can be calculated as follows:

$$SNR\left(\text{dB}\right) = -10 \times \log_{10}\left(MSE_{VAL} \times \frac{1.5523}{2^{18}}\right) \quad (4)$$

where:
1.5523 is a coefficient related to the 10BASE-T1L modulation and symbol coding.
2^{18} is a coefficient coming from the implementation of the on-chip logic mapping the 16-bit register to a useful range.

Table 27. Link Quality vs. MSE Register Value

Link Quality	SNR (dB)	MSE Register Value Range (hex)	BER
Poor	<19.5	>0x0766	$>10^{-8}$
Marginal	19.5 to 20.5	0x05E1 to 0x0766	10^{-8} to 10^{-10}
Good	>20.5	<0x05E1	$<10^{-10}$

Table 28. Signal Quality Indicator vs. MSE Register Value

SQI	SNR (dB)	MSE Register Value Range (hex)	BER
0	<18	>0x0A74	$>10^{-7}$
1	18 to 19	0x084E to 0x0A74	$>10^{-7}$
2	19 to 20	0x0698 to 0x084E	10^{-9} to 10^{-7}
3	20 to 21	0x053D to 0x0698	10^{-11} to 10^{-9}
4	21 to 22	0x0429 to 0x053D	10^{-14} to 10^{-11}
5	22 to 23	0x034E to 0x0429	$<10^{-14}$
6	23 to 24	0x02A0 to 0x034E	$<10^{-14}$
7	>24	<0x02A0	$<10^{-14}$

PHY Slicer Spikes and Errors

The MSE quantity provides an important tool to evaluate the link quality and the effect of noise on the performance of the 10BASE-T1L link. However, given that the MSE is taken as an average value over a period, in cases where the interference is a short transient, the value of the MSE may not reflect this. Yet, there may be enough affectation on the received symbols to produce packet errors.

For this type of transient interference, the ADIN1100, ADIN1101, ADIN1110, ADIN1111, and ADIN2111 include indicators that keep track of the maximum slicer input error and the number of error spikes at the input of the slicer. These indicators also offer the advantage that can be read while there is a 10BASE-T1L link and normal data flow. Thus, these indicators can be utilized to track the link integrity before a hard fault occurs.

Slicer Maximum Absolute Error

As noted in the Mean Squared Error at PHY Slicer section, after the received analog signal is processed, the slicer makes the decision whether the received signal corresponds to a +1, 0, or −1 (PAM3 symbol). For instance, a processed received signal may have a value of 0.8. Thus, the slicer outputs a +1 symbol, given that 0.8 is closer to +1 than to 0 or −1. The closer the processed signal is to the ideal symbol, the more reliable the communication is.

Figure 21 shows the received processed signals at the input of the slicer and the corresponding ideal symbols at the output of the slicer. Notice that the signal marked as 3 has a value of 0.4. Therefore, the slicer outputs a 0 symbol and the actual error is 0.4. If the error is greater than 0.5, the received signal is closer to a +1 symbol than to its ideal 0 symbol. Thus, the slicer interprets the symbol as a +1, producing a bit error in the received frame.

The slicer maximum absolute error must always be less than a value of 0.5. Values close to 0.5 or greater than 0.5 indicate that the received signal integrity has been affected.

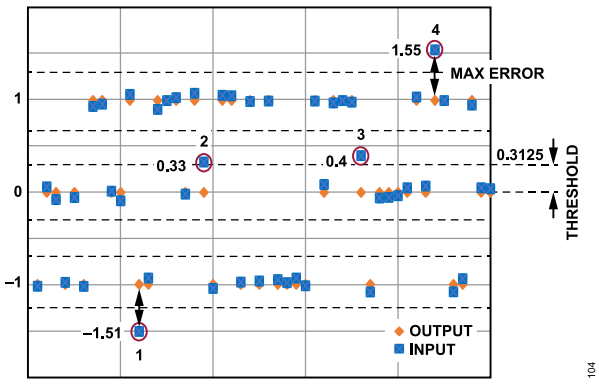

Figure 21. Maximum Slicer Input Error

This maximum error can be tracked over time, before it reaches 0.5, to provide an early indication of link degradation.

Slicer Error Spike Counter

In addition to the maximum slicer absolute error, which only tracks the absolute error of the most deviated symbol, the ADIN1100, ADIN1101, ADIN1110, ADIN1111, and ADIN2111 keep track of the number of received symbols with an absolute error greater than a

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threshold. This counter is called the slicer error spike counter. The slicer error spike counter tracks the number of received symbols with an absolute error above 0.3125 threshold.

Figure 21 shows four signals at the input of the slicer, with errors greater than the 0.3125 threshold. Thus, the slicer error spike counter reports a count of four.

Notice that the threshold (0.3125) has been chosen in a way to provide enough headroom for spikes to be detected before they can produce bit errors.

Relevant Register Information

Table 29 shows the relevant register information. The slicer error spike counter is stored in a 16-bit unsigned format. Therefore, its value is the direct read value from the corresponding register. Reading both registers clears their values and the detection re-starts.

The slicer input maximum absolute error can be converted to symbol units as follows:

$$SlicerMaxAbsError = \frac{SLCR\_ERR\_MAX\_ABS\_VAL}{4096} \quad (5)$$

Register Configuration

To perform register configuration, follow these steps:

1. Write a 0x2 to the SPIKE_CNTRS_CNTRL register.
2. Write a 0x2 to the MAX_ABS_VALS_CNTRL register.
3. Read the SLCR_ERR_MAX_ABS_VAL register, which corresponds to the slicer maximum error.
4. Read the SLCR_ERR_SPIKE_CNT register, which corresponds to the slicer error spike counter.

Perform Step 3 and Step 4 before any test to make sure that the spike counter and maximum absolute errors are cleared. This action is particularly useful while performing tests such as electromagnetic compliance because it is desired to isolate results in pretest and during test.

Table 29. Registers to the Slicer Spike and Error Counters

Register Name	Device Address	Register Address	Description
SLCR_ERR_MAX_ABS_VAL	0x01	0x8308	Slicer maximum absolute error. Latches the value of SLCR_IN_MAX_ABS_VAL.
SLCR_ERR_SPIKE_CNT	0x01	0x8305	Slicer error spike counter. Latches the value of SLCR_IN_SPIKE_CNT.
SPIKE_CNTRS_CNTRL	0x01	0x800E	Specifies whether the spike counters are held when there is no link.
MAX_ABS_VALS_CNTRL	0x01	0x800F	Specifies whether the maximum values are held when there is no link.

The information from the registers in Table 29 can be color coded in a simplified way to provide relevant diagnostics to the end user. A recommended interpretation is explained in Table 30.

Table 30. Link Quality Indication Using Slicer Error Spike Counter and Slicer Maximum Error

Link Quality	Color Indication	Conditions
Poor	Red	Slicer error spike counter > 0 Slicer maximum absolute error ≥ 0.5
Marginal	Yellow	Slicer error spike counter > 0 0.3125 ≤ slicer maximum absolute error < 0.5
Good	Green	Slicer error spike counter = 0 Slicer maximum absolute error < 0.3125

APPLICATIONS INFORMATION

SYSTEM LEVEL POWER MANAGEMENT

Transmit Level = 1.0 V p-p

The 1.0 V p-p transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. This mode supports intrinsic safe applications.

For applications where the ADIN1100 must operate in 1.0 V p-p transmit operating mode, the RXD_0/$\overline{\text{TX2P4\_EN}}$ pin must be tied high via a 4.7 kΩ resistor (see Figure 22). This configuration forces the ADIN1100 to only operate in 1.0 V p-p transmit operating mode and enables the ADIN1100 to operate from a signal supply voltage at a lower voltage rail (for example, 1.8 V), allowing the user to minimize power dissipation in the system.

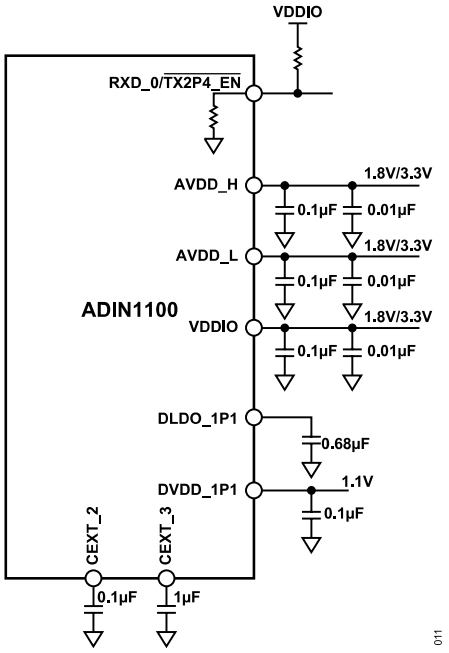


Figure 22. Supplies and Capacitors for Forced 1 V p-p Transmit Mode

Transmit Level = 2.4 V p-p

The higher transmit operating mode of 2.4 V p-p supports trunk applications and requires a higher AVDD_H supply voltage of 3.3 V. This mode can be used for longer cable lengths in industrial Ethernet environments with high noise levels.

For the ADIN1100 to be able to operate at 2.4 V p-p, the RXD_0/$\overline{\text{TX2P4\_EN}}$ pin must be held low (pin has an internal pull-down resistor). This mode of operation still allows the 1.0 V p-p operating mode to be selected via MDIO or via autonegotiation.

Multiple Supplies Configuration

Figure 23 shows an overview of the proposed power configuration. Note that this configuration requires that AVDD_H = 3.3 V even if the link is established in 1.0 V p-p transmit operating mode via MDIO or autonegotiation.

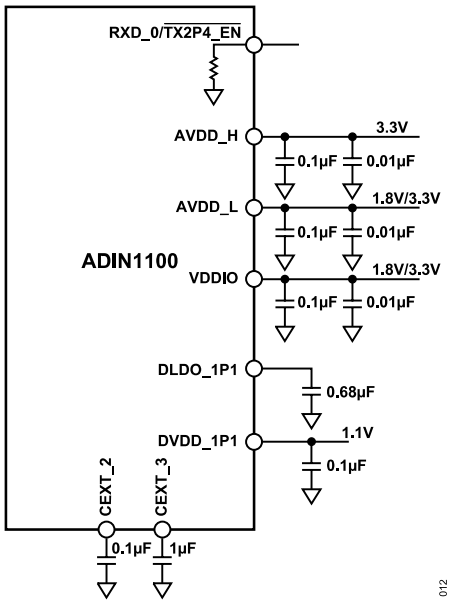


Figure 23. Supplies and Capacitors for Multiple Supply 2.4 V p-p and 1.0 V p-p Transmit Mode

Single-Supply Configuration

For single-supply operation, the same rail can be used to supply the ADIN1100 AVDD_H, AVDD_L, and VDDIO supply rails. The DVDD_1P1 1.1 V rail can be derived internally or alternatively provided by an external 1.1 V rail. This configuration is shown in Figure 24.

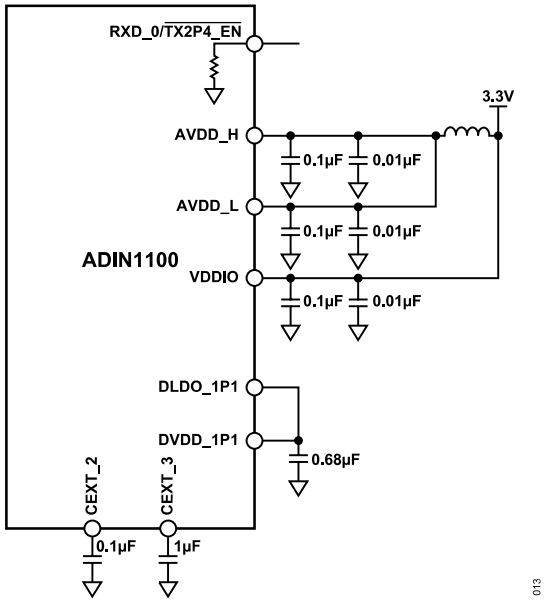


Figure 24. Supplies and Capacitors for Single-Supply 2.4 V p-p Transmit Mode

APPLICATIONS INFORMATION

LED CIRCUIT EXAMPLES

The LED_0 and LED_1 pins can be used in various circuit configurations depending on the LED polarity mode selected (see the LED Polarity Register section). The circuits described in the following sections provide examples for three polarity modes that are available for each LED.

- Autosense (default)
- Active high
- Active low

The output current for the LED_0 and LED_1 pins is 8 mA with a VDDIO = 3.3 V (see the Specifications section for details). For higher current requirements, consider using the circuit described in the Transistor Controlled LED section.

Active High LED Polarity

In active high configuration, the LED_x pin can drive an external LED from the anode side. Select the R0 and R1 resistors to control the LED current (refer to the LED specifications in Table 1 for information). External pull-down resistors (R_{PD0}, R_{PD1}) with a value of 4.7 kΩ are recommended.

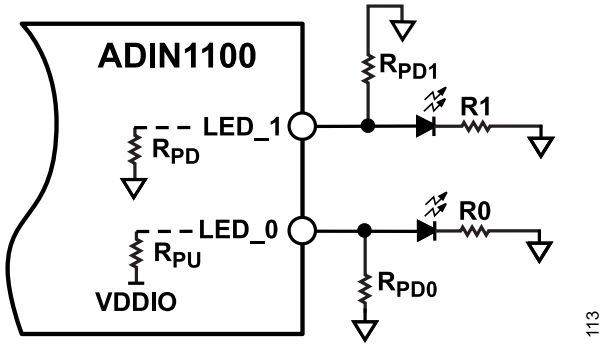


Figure 25. Active High LED Polarity Configuration

Active Low LED Polarity

In active low configuration, the LED_x pin can drive an external LED from the cathode side. Select the R0 and R1 resistors to control the LED current (refer to the LED specifications in Table 1 for information). External pull-up resistors (R_{PU0}, R_{PU1}) with a value of 4.7 kΩ are recommended.

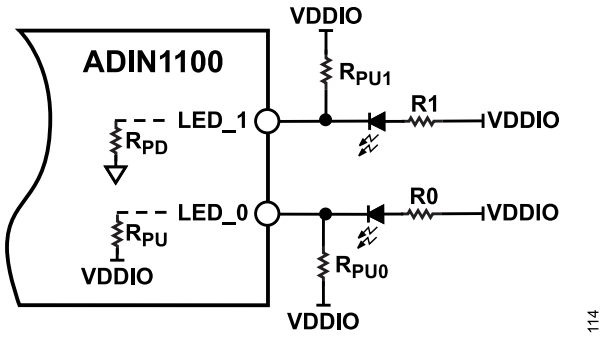


Figure 26. Active Low LED Polarity Configuration

Transistor Controlled LED

The following circuit displays a typical configuration where the LED current required is higher than what the LED_0 and LED_1 pins can supply. The circuit operates using the active high LED mode. An external transistor such as an N channel MOSFET transistor can be used. The transistor must be selected so that the gate input capacitance is not sinking current above the maximum rating of the LED_x pin during the actuation. Refer to the transistor technical specifications for information. If required, the inrush current can be reduced by placing a resistance between the transistor gate and the ADIN1100 pin and/or adding a parallel capacitor between the GND and the LED_x pin. The additional resistor and capacitor values must be defined based on the transistor selection.

Select the R0 and R1 resistors to control the LED current (refer to the selected LED and transistor specifications of the manufacturer for information).

External pull-down resistors (R_{PD0}, R_{PD1}) with a value of 4.7 kΩ are recommended. In Figure 27, VCC is the power supply used to supply the LEDs.

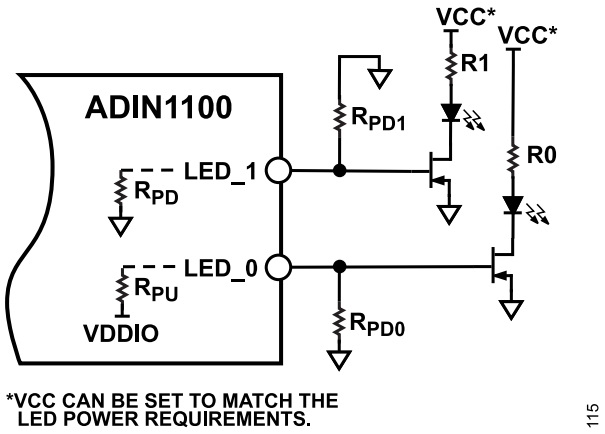


Figure 27. Transistor Controlled LED Configuration

APPLICATIONS INFORMATION

Autosense Polarity

In autosense mode, the polarity of the LED is automatically detected during power-up, hardware reset, or software reset. LED_0 (internal pull-up) and LED_1 (internal pull-down) have different autosense behaviors due to their internal pull-up and pull-down configurations. Use one of the configurations described in the Active High LED Polarity, Active Low LED Polarity, and Transistor Controlled LED sections so that the two LEDs can be controlled the same way.

COMPONENT RECOMMENDATIONS

The ADIN1100 requires an external 25 MHz or 50 MHz clock, which can be sourced from an external crystal oscillator (25 MHz) or an external single-ended clock (25 MHz or 50 MHz). The RMII requires an external 50 MHz clock as described in the External 50 MHz Clock Input for RMII Mode section.

The signal voltage on the XTAL_I/CLK_IN pin (V_{CLK_IN}) must be a sine or filtered square wave signal with a peak-to-peak voltage range from 0.8 V to 2.5 V. For the single-ended clock option, a V_{CLK_IN} with a 1.0 V p-p swing is recommended to achieve best performance.

Various circuit configurations are proposed in the following sections. A common circuit topology can be used across these options with a change to the passive component values.

Note that during normal operation, a 25 MHz reference clock generated from the external clock source input (crystal, 25 MHz or 50 MHz clock) is provided on the CLK25_REF output pin. This pin can be used as a reference clock for other circuits, such as another 10BASE-T1L device. CLK25_REF is disabled in reset mode.

External Crystal Oscillator for RMII and RGMII Modes

The typical connection for an external crystal (XTAL) is shown in Figure 28.

To ensure minimum current consumption and to minimize stray capacitance, make connections between the crystal, capacitors, and ground as close to the ADIN1100 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

The crystal load capacitance (C_L) is defined by the crystal vendor. C_{PCB1} and C_{PCB2} are the parasitic capacitance between the XTAL_I/CLK_IN and XTAL_O tracks and the ground plane beneath, respectively. C_{X1} and C_{X2} are the two external load capacitors required for the oscillator to operate.

Assuming the following:

- $C_{PCB1} \approx C_{PCB2} \approx C_{PCBx}$
- $C_{X1} \approx C_{X2} \approx C_{Xx}$

Then, $C_{Xx} = 2 \times C_L - C_{PCBx} - 3$ pF

Choose precision capacitors for C_{Xx} with low appreciable temperature coefficient to minimize frequency errors.

To ensure minimum current consumption and to minimize stray capacitance, make the connections between the crystal, capacitors, and ground as close to the ADIN1100 as possible.

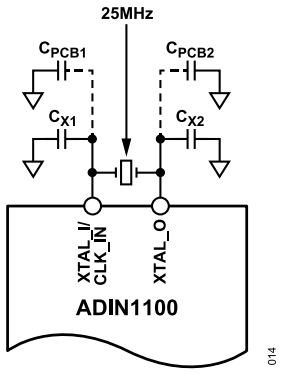


Figure 28. Crystal Oscillator Connection

External 25 MHz Clock Input for MII and RGMII Modes

A single-ended 25 MHz reference clock on XTAL_I/CLK_IN can be used for MII or RGMII mode. The clock source must be dc-coupled with the ADIN1100 XTAL_I/CLK_IN pin input, and the XTAL_O pin must be left open circuit.

With 0.8 V ≤ V_{CLK_IN} p-p ≤ 2.5 V, the following results:

- For 0.8 V ≤ V_S p-p ≤ 1.0 V, the following is true:
  - R1 = 50 Ω
  - R2 is not required
- For 1.0 V < V_S p-p < 1.8 V, the following is true:
  - For best performance, set V_{CLK_IN} to 1.0 V p-p
  - 500 Ω ≤ R1 ≤ 2 kΩ
  - 1 kΩ ≤ R2 ≤ 2 kΩ
  - V_S p-p – V_{CLK_IN} p-p > 0.2 V
  - $R2 = \frac{V_{CLK\_IN}\,p-p \times R1}{V_S\,p-p - V_{CLK\_IN}\,p-p}$
- For 1.8 V ≤ V_S p-p, the following is true:
  - R1 = 2 kΩ
  - R2 = 2 kΩ

APPLICATIONS INFORMATION

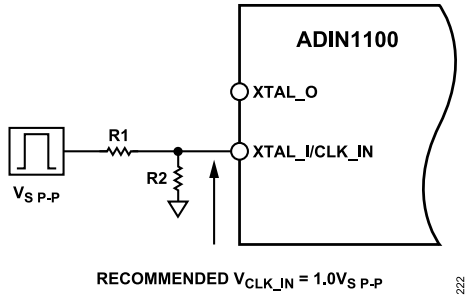


Figure 29. External 25 MHz Clock Input Circuit for MII and RGMII Modes

Table 31. Recommended R1 and R2 Values for Different V_S p-p Values

V_S (V p-p)	R1	R2
1.0	50 Ω	Not applicable
1.2	500 Ω	2.5 kΩ
1.8	2 kΩ	2 kΩ
2.2	2 kΩ	2 kΩ
2.5	2 kΩ	2 kΩ
2.8	2 kΩ	2 kΩ
3.0	2 kΩ	2 kΩ
3.3	2 kΩ	2 kΩ

External 50 MHz Clock Input for RMII Mode

RMII mode requires a single-ended 50 MHz reference clock signal on XTAL/CLK_IN with the XTAL_O pin left open circuit.

The PCB parasitic impedance requires particular attention, and it is recommended to match the clock trace lengths between the ADIN1100 and the external MAC (for example, the meandered trace) for RMII timing purposes.

For best performance, set the ADIN1100 V_{CLK_IN} signal to 1.0 V p-p.

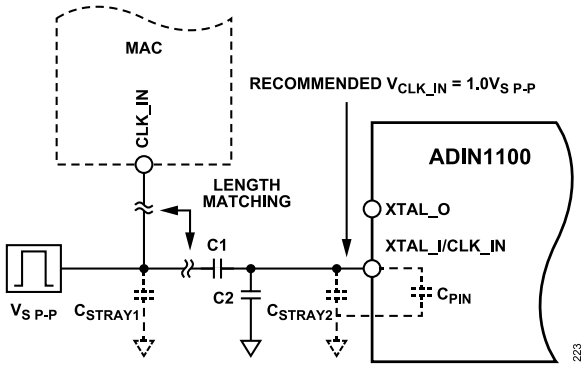


Figure 30. External 50 MHz Clock Input Circuit for RMII Mode

For 0.8 V ≤ V_S p-p ≤ 1 V (dc coupling), the following results:

- C1 = 50 Ω (replace capacitor with resistor)
- C2 not required

For V_S p-p > 1.0 V (ac coupling) and C1 and C2 placed near the ADIN1100 XTAL_I/CLK_IN pin, the following results:

- C1 = 70 pF maximum
- C2 = 10 pF
- C_{PIN} = 3 pF (ADIN1100 pin capacitance)
- C_{STRAY2} ≈ 0 pF
- V_S p-p – V_{CLK_IN} p-p > 0.2 V
- $$C1 = \frac{V_{CLK\_IN} \times (C2 + C_{STRAY2} + C_{PIN})}{V_S - V_{CLK\_IN}}$$

Table 32. C1 and C2 Values for Different V_S p-p Values with V_{CLK_IN} = 1 V p-p

V_S V p-p	C2 (pF)	C1
1.0	Not applicable	50 Ω
1.2	10	68 pF
1.8	10	18 pF
2.2	10	12 pF
2.5	10	10 pF
2.8	10	8.2 pF
3.0	10	8.2 pF
3.3	10	8.2 pF

The capacitor tolerance from the manufacturer must be included in the calculations to provide a reasonable margin with regard to the V_{CLK_IN} target voltage.

Note that additional filtering can be required for the external MAC module. The selected clock source must be able to supply the current required by the circuit.

PCB Parasitic Capacitance Considerations

The parasitic capacitance of the clock traces can have a nonnegligible impact on the signal. The PCB stack and the trace impedance must be selected carefully to reduce parasitic impedance and provide the best timing performance, especially if the RMII is selected (50 MHz clock).

Considering the ac coupling RMII scenario described in the External 50 MHz Clock Input for RMII Mode section, Table 33 displays some basic calculations of the PCB parasitic capacitance using the following PCB parameters:

- Transmit line type: Microstrip Layer 1 and Layer 2
- Clock trace width: W = 127 µm (5 mils)
- PCB L1 copper foil thickness after plating: T = 35 µm (1.38 mils)
- L1 to L2 ground plane distance: H = 0.116 mm (4.55 mils)
- Substrate relative permittivity: ε_r = 4.6 (FR4)

In addition, see the IPC-2141 standard for models and guidelines.

Table 33. Trace Parasitic Capacitance Examples

Total Clock Trace Length (cm)	Clock Trace Stray Capacitance (pF)
1	~1

APPLICATIONS INFORMATION

Table 33. Trace Parasitic Capacitance Examples (Continued)

Total Clock Trace Length (cm)	Clock Trace Stray Capacitance (pF)
2	~2
5	~5

ELECTROMAGNETIC COMPATIBILITY (EMC) AND ELECTROMAGNETIC IMMUNITY (EMI)

The ADIN1100 was tested at the system level for EMC and EMI. Table 34 summarizes the results.

Table 34. EMC/EMI Tests Conducted on ADIN1100 at System Level

EMC/EMI Test	Withstand Threshold/Class
IEC 61000-4-4 EFT	±4 kV
IEC 61000-4-2 ESD (contact discharge)	±4 kV
IEC 61000-4-2 ESD (air discharge)	±8 kV
IEC 61000-4-5 Surge	±4 kV
IEC 61000-4-6 Conducted Immunity	10 V/m
IEC 61000-4-3 Radiated Immunity	Class A
EN 55032 Radiated Emissions	Class B

MDIO INTERFACE

The management interface provides a 2-wire serial interface (MDIO) between a host controller (such as micro-controller or an external MAC chip) and the ADIN1100, allowing read and write operations in the management registers.

The management interface of the ADIN1100 is compatible with both IEEE Standard 802.3 Clause 22 and IEEE Standard 802.3 Clause 45.

The hardware configuration pins determine the default value of some registers after power-up, hardware reset, or software reset. For those registers, the reset value referenced in the register bit description tables is listed as pin dependent. This dependency allows the ADIN1100 to be configured in hardware without the need for software operations over the MDIO interface (unmanaged application).

The Hardware Configuration Pins section provides full details on configuration pin setup for managed and unmanaged applications.

The access permissions of the registers are as follows:

- R/W: read/write
- R: read only
- R LL: read only, latch low
- R LH: read only, latch high
- R/W SC: read/write, self clear
- R SC: read only, self clear

CLAUSE 22

IEEE Standard 802.3 Clause 22 allows access to up to 32 registers in 32 different PHY addresses.

The IEEE Clause 22 MMD register access format is shown in Table 35 and Table 36.

Table 35. Clause 22 Frame Format

MSB					LSB
D31 to D30	**D29 to D28**	**D27 to D23**	**D22 to D18**	**D17 to D16**	**D15 to D0**
ST	OP	PHYADR	REGAD	TA	Data

Table 36. Clause 22 Input Register Decode

Bit	Description
ST	2-bit start of frame (01 for Clause 22)
OP	2-bit operation code 01: write 10: read
PHYADR	5-bit PHY address
REGAD	5-bit register address
TA	2-bit turn around field used to avoid contention during a read transition, 2-bit time spacing between register address field and data field
Data	16-bit data, MSB first

MDIO INTERFACE

CLAUSE 45

The clause 45 registers are made up of four device address groupings (see Table 37) based on the MDIO manageable device (MMD). Within each device address space, IEEE standard registers are located in register addresses between 0x0000 and 0x7FFF and vendor specific registers are located in register addresses from 0x8000 to 0xFFFF.

This setup allows access to up to 32 PHYs consisting of up to 32 MMDs through a single MDIO interface.

The IEEE Clause 45 MMD register access format is shown in Table 38 and Table 39.

Clause 45 operations differ from Clause 22 operations where a single frame specifies the register address and data to read or write. In Clause 45, a first frame is sent to specify the device address and register address to access. A second frame is then sent to perform the read or write operation on the selected device address and register specified in the first frame.

Table 37. Register Groupings

Device Address	MMD Name
0x01	PMA and physical medium dependent (PMD)
0x03	PCS
0x07	Autonegotiation
0x1E	Vendor Specific 1
0x1F	Vendor Specific 2

Table 38. Clause 45 Frame Format

MSB					LSB
D31 to D30	D29 to D28	D27 to D23	D22 to D18	D17 to D16	D15 to D0
ST	OP	PHYADR	DEVAD	TA	Address/data

Table 39. Clause 45 Input Register Decode

Bit	Description
ST	2-bit start of frame (00 for Clause 45)
OP	2-bit operation code 00: address 01: write 11: read 10: read + address
PHYADR	5-bit PHY address
DEVAD	5-bit device address
TA	2-bit turn around field used to avoid contention during a read transition, 2-bit time spacing between register address field and data field
Address/Data	16-bit register address/data

MDIO INTERFACE

RECOMMENDED REGISTER OPERATION

Many of the ADIN1100 registers are defined and compliant with the IEEE 802.3 standard. The register behaviors defined by the standard are not always obvious and are described in the Latch Low Registers, IEEE Duplicated Registers, and Read Modify Write Operation sections, including the recommended operation and use of the registers.

Latch Low Registers

The IEEE Standard 802.3-2018 requires certain MDIO accessible registers to exhibit latch low behavior. This behavior allows software that only intermittently reads these registers to detect conditions that may be transitory or short lived. For example, the AN_LINK_STATUS bit is required to latch low. When the device exits from a reset or power-down state, the latching condition is not active and the value of the AN_LINK_STATUS bit reflects the current status of the link. However, if the link comes up and then drops, the latching condition becomes active. In this case, the AN_LINK_STATUS bit reads as 0 even if the link has come back up again in the interim. The latching condition is only cleared after the AN_LINK_STATUS bit is read to ensure that software has had the opportunity to observe that the link dropped.

This latch low behavior means that the software must perform two reads of the AN_LINK_STATUS bit back to back to determine the current status of the link. The first read is needed to clear any active latching condition.

It is important that the software take account of the interaction between MDIO accessible bits that share a register address. For example, the AN_PAGE_RX and AN_LINK_STATUS bits reside at the same register address. As a result, reading the AN_PAGE_RX bit clears any active latching condition associated with the AN_LINK_STATUS bit.

IEEE Duplicated Registers

IEEE Standard 802.3-2018 covers a wide range of definitions and speeds from 10 Mbps to 40 Gbps and higher, and includes an extensive number of clauses. Many of the registers defined by this standard are associated with various clauses, and different PHYs may include different clauses and/or combinations of clauses. Thus, the registers for common functions like software reset, software power-down, and loopback tend to be implemented in multiple clauses.

In the ADIN1100, the physical implementation of these registers is in a single location, but they can be accessed at multiple addresses. For example, the software reset bit can be read or written in all the IEEE MMD locations and vendor specific register locations listed in Table 40.

Table 40. Software Reset Bit Access in IEEE MMD Locations

Register Name	Device Address	Register Address	Bit Name	Bit
PMA/PMD Control 1 (IEEE 802.3)	0x01	0x0000	Reset (IEEE 802.3)	15
10BASE-T1L PMA Control (IEEE 802.3.cg)	0x01	0x08F6	PMA reset (IEEE 802.3.cg)	15
PCS Control 1 (IEEE 802.3)	0x03	0x0000	Reset (IEEE 802.3)	15
10BASE-T1L PCS Control (IEEE 802.3.cg)	0x03	0x08E6	PCS reset (IEEE 802.3.cg)	15
Software Reset (ADIN1100)	0x1E	0x8810	CRSM_SFT_RST (ADIN1100)	0

In this example, these locations are the PMA/PMD, PCS, autonegotiation, and Vendor Specific 1 device address locations (per Table 37).

The ADIN1100 has multiple address locations for the same register to match the IEEE standard.

The ADIN1100 data sheet only mentions a single recommended address location for each of these IEEE registers to simplify the operation and use of the device. In general, the registers introduced in the 802.3cg (10BASE-T1L) section of the standard are recommended over older (equivalent) registers. Registers in a vendor specific address are recommended, in particular where a register brings a number of useful IEEE register bits into a single register address. The ADIN1100 correctly responds to register accesses to all the IEEE register address locations covered by the 10BASE-T1L standard when the start-up sequence is complete after power-up, hardware reset, or software reset.

Read Modify Write Operation

It is strongly recommended that all register write operations be performed as read modify write, especially when modifying individual register bits. If this is not followed, the value of register bits can be inadvertently changed.

REGISTER SUMMARY

ETHERNET CLAUSE 22 REGISTER DETAILS

Table 41. ADIN1100 Register Summary

Address	Name	Description	Reset	Access
0x0	MI_CONTROL	MII Control Register.	0x1100	R/W
0x1	MI_STATUS	MII Status Register.	0x1009	R
0x2	MI_PHY_ID1	PHY Identifier 1 Register.	0x0283	R
0x3	MI_PHY_ID2	PHY Identifier 2 Register.	0xBC81	R
0xD	MMD_ACCESS_CNTRL	MMD Access Control.	0x0000	R/W
0xE	MMD_ACCESS	MMD Access.	0x0000	R/W

MII Control Register

Address: 0x0, Reset: 0x1100, Name: MI_CONTROL

This address corresponds to the MII control register specified in Clause 22.2.4.1 of Standard 802.3.

Table 42. Bit Descriptions for MI_CONTROL

Bits	Bit Name	Description	Reset	Access
15	MI_SFT_RST	Software Reset. The software reset bit allows a software reset cycle to be initiated. Mirrors CRSM_SFT_RST.	0x0	R/W SC
14	MI_LOOPBACK	Local Loopback (PCS). The loopback bit allows the PHY loopback mode to be engaged. Mirrors LB_PCS_EN.	0x0	R/W
13	MI_SPEED_SEL_LSB	MII Speed Selection LSB. See MI_SPEED_SEL_MSB.	0x0	R
12	MI_AN_EN	Autonegotiation Enable. Use the AN_FRC_MODE_EN bit to enable forced link configuration mode. Mirrors AN_EN. 0: disable autonegotiation. 1: enable autonegotiation.	0x1	R
11	MI_SFT_PD	Software Power-Down. The software power-down bit allows the PHY to be placed in software power-down mode. In this mode, most of the PHY circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via the RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$ pin, which allows the PHY to be held in reset until an appropriate software initialization has been performed. Mirrors CRSM_SFT_PD.	Pin dependent	R/W
10	MI_ISOLATE	MII Isolate. The isolate bit allows the PHY to be isolated from the MII.	0x0	R/W
9	RESERVED	Reserved.	0x0	R/W SC
8	MI_FULL_DUPLEX	MII Full Duplex. The duplex mode bit cannot be written and always reads as 1 because the PHY is only able to operate in full duplex mode.	0x1	R
7	MI_COLTEST	MII Collision Test. The collision test bit cannot be written and always reads as 0 because the PHY is only able to operate in full duplex mode, and does not have a collision detect MII (COL) pin.	0x0	R
6	MI_SPEED_SEL_MSB	MII Speed Selection MSB. The speed selection MSB and LSB bits cannot be written and always reads as 00 because the PHY is only able to operate at 10 Mbps.	0x0	R
5	MI_UNIDIR_EN	MII Unidirectional Enable. The unidirectional enable bit cannot be written and always reads as 0 because the PHY does not have the ability to transmit data from the MII regardless of whether it has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

MII Status Register

Address: 0x1, Reset: 0x1009, Name: MI_STATUS

This address corresponds to the MII status register specified in Clause 22.2.4.2 of Standard 802.3.

REGISTER SUMMARY

Table 43. Bit Descriptions for MI_STATUS

Bits	Bit Name	Description	Reset	Access
15	MI_T4_SPRT	100BASE-T4 Ability. The 100BASE-T4 ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
14	MI_FD100_SPRT	Full Duplex 100BASE-X Ability. The 100BASE-X full duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
13	MI_HD100_SPRT	Half-Duplex 100BASE-X Ability. The 100BASE-X half-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
12	MI_FD10_SPRT	Full Duplex 10 Mbps Ability. The 10 Mbps full duplex ability bit indicates that the PHY supports this technology.	0x1	R
11	MI_HD10_SPRT	Half-Duplex 10 Mbps Ability. The 10 Mbps half-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
10	MI_FD_T2_SPRT	Full Duplex 100BASE-T2 Ability. The 100BASE-T2 full duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
9	MI_HD_T2_SPRT	Half-Duplex 100BASE-T2- Ability. The 100BASE-T2 half-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
8	MI_EXT_STAT_SPRT	Extended Status Support. The extended status support bit always reads as 0 to indicate that the PHY does not provide extended status information in Register 0xF.	0x0	R
7	MI_UNIDIR_ABLE	Unidirectional Ability. The unidirectional ability bit always reads as 0 to indicate that the PHY can only transmit data from the MII when it has determined that a valid link has been established.	0x0	R
6	MI_MF_PREAM_SUP_ABLE	Management Preamble Suppression Ability. The management frame preamble suppression ability bit always reads as 0 to indicate that the PHY is not able to receive management frames that are not preceded by the preamble pattern.	0x0	R
5	MI_AN_COMPLETE	Autonegotiation Complete. The autonegotiation complete bit indicates that the autonegotiation process has been completed and the PHY link is up. Mirrors AN_COMPLETE.	0x0	R
4	MI_REM_FLT	Remote Fault. The remote fault bit always reads as 0 because the PHY has no provision for remote fault detection.	0x0	R LH
3	MI_AN_ABLE	Autonegotiation Ability. The autonegotiation ability bit always reads as 1 indicating that the PHY has the ability to perform autonegotiation. Mirrors AN_ABLE.	0x1	R
2	MI_LINK_STAT_LAT	Link Status. The link status bit uses a latch low functionality as described in IEEE Standard 802.3 Subclause 45.2.7.20.5. If the link status value is fail, this bit clears and remains cleared until the latching is cleared when the bit is read. Mirrors 7.513.2 (AN_LINK_STATUS).	0x0	R LL
1	MI_JABBER_DET	MII Jabber Detect. The jabber detect bit always reads as 0 because the 10BASE-T1L PHY does not incorporate a jabber detect function.	0x0	R LH
0	MI_EXT_CAPABLE	MII Extended Capability. The extended capability bit always reads as 1, indicating that the PHY provides an extended set of capabilities that can be accessed through the extended register set. The extended register set consists of all of the management registers except 0x0, 0x1, and 0xF.	0x1	R

PHY Identifier 1 Register

Address: 0x2, Reset: 0x0283, Name: MI_PHY_ID1

The PHY Identifier 1 address allows 16 bits of the OUI to be observed.

Table 44. Bit Descriptions for MI_PHY_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MI_PHY_ID1	The PHY Identifier 1 address allows 16 bits of the OUI to be observed.	0x283	R

PHY Identifier 2 Register

Address: 0x3, Reset: 0xBC81, Name: MI_PHY_ID2

The PHY Identifier 2 address allows six bits of the OUI, and the model and revision number to be observed.

REGISTER SUMMARY

Table 45. Bit Descriptions for MI_PHY_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MI_PHY_ID2_OUI	OUI, Bits[7:2].	0x2F	R
[9:4]	MI_MODEL_NUM	Model Number.	0x8	R
[3:0]	MI_REV_NUM	Revision Number.	0x1	R

MMD Access Control Register

Address: 0xD, Reset: 0x0000, Name: MMD_ACCESS_CNTRL

This address corresponds to the MMD access control register specified in Clause 22.2.4.3.11 of IEEE Standard 802.3-2018.

Table 46. Bit Descriptions for MMD_ACCESS_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD_ACR_FUNCTION	Function. The function bits select the type of MMD access on accesses to the MMD_ACCESS register. 00: address. 01: data, no post increment. 10: data, post increment on reads and writes. 11: data, post increment on writes only.	0x0	R/W
[13:5]	RESERVED	Reserved.	0x0	R
[4:0]	MMD_ACR_DEVAD	Device Address. The value in this bit directs any accesses to the MMD_ACCESS register to the selected MMD.	0x0	R/W

MMD Access Register

Address: 0xE, Reset: 0x0000, Name: MMD_ACCESS

This address corresponds to the MMD access address data register specified in Clause 22.2.4.3.12 of IEEE Standard 802.3-2018.

The MMD_ACCESS register is used in conjunction with the MMD_ACCESS_CNTRL register to provide access to the MMD address space using the interface and mechanisms defined in Clause 22.2.4.

Table 47. Bit Descriptions for MMD_ACCESS

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD_ACCESS	Access Address. This address corresponds to the MMD access address data register specified in Clause 22.2.4.3.12 of IEEE Standard 802.3-2018. The MMD_ACCESS register is used in conjunction with the MMD_ACCESS_CNTRL register to provide access to the MMD address space using the interface and mechanisms defined in Clause 22.2.4.	0x0	R/W

ETHERNET CLAUSE 45 REGISTER DETAILS

Table 48. Ethernet Clause 45 Register Summary

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x0000	PMA_PMD_CNTRL1	PMA/PMD Control 1 Register.	0x0000	R/W
0x01	0x0001	PMA_PMD_STAT1	PMA/PMD Status 1 Register.	0x0002	R
0x01	0x0005	PMA_PMD_DEVS_IN_PKG1	PMA/PMD MMD Devices in Package 1.	0x008B	R
0x01	0x0006	PMA_PMD_DEVS_IN_PKG2	PMA/PMD MMD Devices in Package 2 Register.	0xC000	R
0x01	0x0007	PMA_PMD_CNTRL2	PMA/PMD Control 2 Register.	0x003D	R/W
0x01	0x0008	PMA_PMD_STAT2	PMA/PMD Status 2.	0x8301	R
0x01	0x0009	PMA_PMD_TX_DIS	PMA/PMD Transmit Disable Register.	0x0000	R/W
0x01	0x000B	PMA_PMD_EXT_ABILITY	PMA/PMD Extended Abilities Register.	0x0800	R

REGISTER SUMMARY

Table 48. Ethernet Clause 45 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x0012	PMA_PMD_BT1_ABILITY	BASE-T1 PMA/PMD Extended Ability Register.	0x0004	R
0x01	0x0834	PMA_PMD_BT1_CONTROL	BASE-T1 PMA/PMD Control Register.	0x8002	R/W
0x01	0x08F6	B10L_PMA_CNTRL	10BASE-T1L PMA Control Register.	0x0000	R/W
0x01	0x08F7	B10L_PMA_STAT	10BASE-T1L PMA Status Register.	0x2800	R
0x01	0x08F8	B10L_TEST_MODE_CNTRL	10BASE-T1L Test Mode Control Register.	0x0000	R/W
0x01	0x8302	B10L_PMA_LINK_STAT	10BASE-T1L PMA Link Status Register.	0x0000	R
0x01	0x830B	MSE_VAL	Mean Squared Error (MSE) Value Register.	0x0000	R
0x03	0x0000	PCS_CNTRL1	PCS Control 1 Register.	0x0000	R/W
0x03	0x0001	PCS_STAT1	PCS Status 1 Register.	0x0002	R
0x03	0x0005	PCS_DEVS_IN_PKG1	PCS MMD Devices in Package 1 Register.	0x008B	R
0x03	0x0006	PCS_DEVS_IN_PKG2	PCS MMD Devices in Package 2 Register.	0xC000	R
0x03	0x0008	PCS_STAT2	PCS Status 2 Register.	0x8000	R
0x03	0x08E6	B10L_PCS_CNTRL	10BASE-T1L PCS Control Register.	0x0000	R/W
0x03	0x08E7	B10L_PCS_STAT	10BASE-T1L PCS Status Register.	0x0000	R
0x07	0x0005	AN_DEVS_IN_PKG1	Autonegotiation MMD Devices in Package 1 Register.	0x008B	R
0x07	0x0006	AN_DEVS_IN_PKG2	Autonegotiation MMD Devices in Package 2 Register.	0xC000	R
0x07	0x0200	AN_CONTROL	BASE-T1 Autonegotiation Control Register.	0x1000	R/W
0x07	0x0201	AN_STATUS	BASE-T1 Autonegotiation Status Register.	0x0008	R
0x07	0x0202	AN_ADV_ABILITY_L	BASE-T1 Autonegotiation Advertisement Register, Bits[15:0].	0x0001	R/W
0x07	0x0203	AN_ADV_ABILITY_M	BASE-T1 Autonegotiation Advertisement Register, Bits[31:16].	0x4000	R/W
0x07	0x0204	AN_ADV_ABILITY_H	BASE-T1 Autonegotiation Advertisement Register, Bits[47:32].	0x0000	R/W
0x07	0x0205	AN_LP_ADV_ABILITY_L	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[15:0].	0x0000	R
0x07	0x0206	AN_LP_ADV_ABILITY_M	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[31:16].	0x0000	R
0x07	0x0207	AN_LP_ADV_ABILITY_H	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[47:32].	0x0000	R
0x07	0x0208	AN_NEXT_PAGE_L	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[15:0].	0x2001	R/W
0x07	0x0209	AN_NEXT_PAGE_M	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[31:16].	0x0000	R/W
0x07	0x020A	AN_NEXT_PAGE_H	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[47:32].	0x0000	R/W
0x07	0x020B	AN_LP_NEXT_PAGE_L	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[15:0].	0x0000	R
0x07	0x020C	AN_LP_NEXT_PAGE_M	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[31:16].	0x0000	R
0x07	0x020D	AN_LP_NEXT_PAGE_H	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[47:32].	0x0000	R
0x07	0x020E	AN_B10_ADV_ABILITY	10BASE-T1 Autonegotiation Control Register.	0x8000	R/W
0x07	0x020F	AN_B10_LP_ADV_ABILITY	10BASE-T1 Autonegotiation Status Register.	0x0000	R
0x07	0x8000	AN_FRC_MODE_EN	Autonegotiation Forced Mode Enable Register.	0x0000	R/W
0x07	0x8001	AN_STATUS_EXTRA	Extra Autonegotiation Status Register.	0x0000	R

REGISTER SUMMARY

Table 48. Ethernet Clause 45 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x07	0x8030	AN_PHY_INST_STATUS	PHY Instantaneous Status.	0x0010	R
0x1E	0x0002	MMD1_DEV_ID1	Vendor Specific 1 MMD Identifier High Register.	0x0283	R
0x1E	0x0003	MMD1_DEV_ID2	Vendor Specific 1 MMD Identifier Low Register.	0xBC81	R
0x1E	0x0005	MMD1_DEVS_IN_PKG1	Vendor Specific 1 MMDs in Package Register.	0x008B	R
0x1E	0x0006	MMD1_DEVS_IN_PKG2	Vendor Specific 1 MMDs in Package Register.	0xC000	R
0x1E	0x0008	MMD1_STATUS	Vendor Specific 1 MMD Status Register.	0x8000	R
0x1E	0x0010	CRSM_IRQ_STATUS	System Interrupt Status Register.	0x1000	R
0x1E	0x0020	CRSM_IRQ_MASK	System Interrupt Mask Register.	0x1FFE	R/W
0x1E	0x8810	CRSM_SFT_RST	Software Reset Register.	0x0000	R/W
0x1E	0x8812	CRSM_SFT_PD_CNTRL	Software Power-Down Control Register.	0x0000	R/W
0x1E	0x8814	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset Register.	0x0000	R/W
0x1E	0x8815	CRSM_MAC_IF_RST	PHY MAC Interface Reset Register.	0x0000	R/W
0x1E	0x8818	CRSM_STAT	System Status Register.	0x0000	R
0x1E	0x8819	CRSM_PMG_CNTRL	Clock, Reset, and State Machine (CRSM) Power Management Control Register.	0x0000	R/W
0x1E	0x882B	CRSM_MAC_IF_CFG	MAC Interface Configuration Register.	0x0000	R/W
0x1E	0x882C	CRSM_DIAG_CLK_CTRL	CRSM Diagnostics Clock Control.	0x0002	R/W
0x1E	0x8C22	MGMT_PRT_PKG	Package Configuration Values Register.	0x0000	R
0x1E	0x8C30	MGMT_MDIO_CNTRL	MDIO Control Register.	0x0000	R/W
0x1E	0x8C56	DIGIO_PINMUX	Pin Mux Configuration 1 Register.	0x00FE	R/W
0x1E	0x8C57	DIGIO_PINMUX2	Pin Mux Configuration 2 Register.	0x00FF	R/W
0x1E	0x8C80	LED0_BLINK_TIME_CNTRL	LED_0 On/Off Blink Time Register.	0x3636	R/W
0x1E	0x8C81	LED1_BLINK_TIME_CNTRL	LED_1 On/Off Blink Time Register.	0x3636	R/W
0x1E	0x8C82	LED_CNTRL	LED Control Register.	0x8480	R/W
0x1E	0x8C83	LED_POLARITY	LED Polarity Register.	0x0000	R/W
0x1F	0x0002	MMD2_DEV_ID1	Vendor Specific 2 MMD Identifier High Register.	0x0283	R
0x1F	0x0003	MMD2_DEV_ID2	Vendor Specific 2 MMD Identifier Low Register.	0xBC81	R
0x1F	0x0005	MMD2_DEVS_IN_PKG1	Vendor Specific 2 MMDs in Package Register.	0x008B	R
0x1F	0x0006	MMD2_DEVS_IN_PKG2	Vendor Specific 2 MMDs in Package Register.	0xC000	R
0x1F	0x0008	MMD2_STATUS	Vendor Specific 2 MMD Status Register.	0x8000	R
0x1F	0x0011	PHY_SUBSYS_IRQ_STATUS	PHY Subsystem Interrupt Status Register.	0x0000	R
0x1F	0x0021	PHY_SUBSYS_IRQ_MASK	PHY Subsystem Interrupt Mask Register.	0x2402	R/W
0x1F	0x8001	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x1F	0x8004	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x1F	0x8005	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x1F	0x8008	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x1F	0x8009	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x1F	0x800A	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x1F	0x800B	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R
0x1F	0x800C	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R
0x1F	0x800D	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Count Register.	0x0000	R
0x1F	0x800E	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R

REGISTER SUMMARY

Table 48. Ethernet Clause 45 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x1F	0x800F	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x1F	0x8010	FC_ODD_CNT	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x1F	0x8011	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x1F	0x8013	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x1F	0x8020	FG_EN	Frame Generator Enable Register.	0x0000	R/W
0x1F	0x8021	FG_CNTRL_RSTRT	Frame Generator Control/Restart Register.	0x0001	R/W
0x1F	0x8022	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x1F	0x8023	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x1F	0x8025	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x1F	0x8026	FG_IFG_LEN	Frame Generator Interframe Gap Length Register.	0x000C	R/W
0x1F	0x8027	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W
0x1F	0x8028	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x1F	0x8029	FG_DONE	Frame Generator Done Register.	0x0000	R
0x1F	0x8050	RMII_CFG	RMII Configuration Register.	0x0006	R/W
0x1F	0x8055	MAC_IF_LOOPBACK	MAC Interface Loopbacks Configuration Register.	0x000A	R/W
0x1F	0x805A	MAC_IF_SOP_CNTRL	MAC Start of Packet (SOP) Generation Control Register.	0x001B	R/W

PMA/PMD Control 1 Register

Device Address: 0x01; Register Address: 0x0000, Reset: 0x0000, Name: PMA_PMD_CNTRL1

This address corresponds to PMA/PMD Control Register 1 specified in Clause 45.2.1.1 of Standard 802.3. Note that the reset value of this register is dependent on the hardware configuration pin settings.

Table 49. Bit Descriptions for PMA_PMD_CNTRL1

Bits	Bit Name	Description	Reset	Access
15	PMA_SFT_RST	PMA Software Reset. The PMA software reset bit allows the chip to be reset. When this bit is set, the chip fully initializes, almost equivalent to a hardware reset. This bit is self clearing and returns a value of 1 when a reset is in progress. Otherwise, it returns a value of 0.	0x0	R/W SC
[14:12]	RESERVED	Reserved.	0x0	R
11	PMA_SFT_PD	PMA Software Power-Down. The PMA software power-down bit puts the chip in a lower power mode. In this mode, most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this bit is configurable via the RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$ pin, which allows the chip to be held in power-down mode until an appropriate software initialization is performed.	0x0	R/W
[10:1]	RESERVED	Reserved.	0x0	R
0	LB_PMA_LOC_EN	Enables PMA Local Loopback. When this bit is set to 1, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PMA works in normal mode.	0x0	R/W

PMA/PMD Status 1 Register

Device Address: 0x01; Register Address: 0x0001, Reset: 0x0002, Name: PMA_PMD_STAT1

This address corresponds to PMA/PMD Status Register 1 specified in Clause 45.2.1.2 of Standard 802.3.

REGISTER SUMMARY

Table 50. Bit Descriptions for PMA_PMD_STAT1

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	PMA_LINK_STAT_OK_LL	PMA Link Status. When read as 1, this bit indicates that the link is up. When read as 0, it indicates that the link has dropped since the last time the bit was read.	0x0	R LL
1	PMA_SFT_PD_ABLE	PMA Software Power-Down Able. Indicates that the PMA supports software power-down.	0x1	R
0	RESERVED	Reserved.	0x0	R

PMA/PMD MMD Devices in Package 1 Register

Device Address: 0x01; Register Address: 0x0005, Reset: 0x008B, Name: PMA_PMD_DEVS_IN_PKG1

Table 51. Bit Descriptions for PMA_PMD_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	PMA_PMD_DEVS_IN_PKG1	PMA/PMD MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

PMA/PMD MMD Devices in Package 2 Register

Device Address: 0x01; Register Address: 0x0006, Reset: 0xC000, Name: PMA_PMD_DEVS_IN_PKG2

Table 52. Bit Descriptions for PMA_PMD_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	PMA_PMD_DEVS_IN_PKG2	PMA/PMD MMD Devices in Package 2. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

PMA/PMD Control 2 Register

Device Address: 0x01; Register Address: 0x0007, Reset: 0x003D, Name: PMA_PMD_CNTRL2

Table 53. Bit Descriptions for PMA_PMD_CNTRL2

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:0]	PMA_PMD_TYPE_SEL	PMA/PMD Type Selection. See IEEE Standard 802.3. PMA_PMD_TYPE_SEL is used only when autonegotiation is disabled and forced link configuration mode is enabled. If autonegotiation is enabled, the PHY type is determined by the autonegotiation process itself. Note that for ADIN1100, the only valid value for this bit field is for BASE-T1 PMA/PMD. 0000000: 10GBASE-CX4 PMA/PMD. 0000001: 10GBASE-EW PMA/PMD. 0000010: 10GBASE-LW PMA/PMD. 0000011: 10GBASE-SW PMA/PMD. 0000100: 10GBASE-LX4 PMA/PMD. 0000101: 10GBASE-ER PMA/PMD. 0000110: 10GBASE-LR PMA/PMD. 0000111: 10GBASE-SR PMA/PMD. 0001000: 10GBASE-LRM PMA/PMD. 0001001: 10GBASE-T PMA. 0001010: 10GBASE-KX4 PMA/PMD. 0001011: 10GBASE-KR PMA/PMD. 0001100: 1000BASE-T PMA/PMD. 0001101: 1000BASE-KX PMA/PMD.	0x3D	R/W

REGISTER SUMMARY

Table 53. Bit Descriptions for PMA_PMD_CNTRL2 (Continued)

Bits	Bit Name	Description	Reset	Access
		0001110: 100BASE-TX_PMA/PMD. 0001111: 10BASE-T PMA/PMD. 0010000: 10/1GBASE-PRX-D1. 0010001: 10/1GBASE-PRX-D2. 0010010: 10/1GBASE-PRX-D3. 0010011: 10GBASE-PR-D1. 0010100: 10GBASE-PR-D2. 0010101: 10GBASE-PR-D3. 0010110: 10/1GBASE-PRX-U1. 0010111: 10/1GBASE-PRX-U2. 0011000: 10/1GBASE-PRX-U3. 0011001: 10GBASE-PR-U1. 0011010: 10GBASE-PR-U3. 0011011: reserved. 0011100: 10GBASE-PR-D4. 0011101: 10/1GBASE-PRX-D4. 0011110: 10GBASE-PR-U4. 0011111: 10/1GBASEPRX-U4. 0100000: 40GBASE-KR4 PMA/PMD. 0100001: 40GBASE-CR4 PMA/PMD. 0100010: 40GBASE-SR4 PMA/PMD. 0100011: 40GBASE-LR4 PMA/PMD. 0100100: 40GBASE-FR PMA/PMD. 0100101: 40GBASE-ER4 PMA/PMD. 0100110: 40GBASE-T PMA. 0101000: 100GBASE-CR10 PMA/PMD. 0101001: 100GBASE-SR10 PMA/PMD. 0101010: 100GBASE-LR4 PMA/PMD. 0101011: 100GBASE-ER4 PMA/PMD. 0101100: 100GBASE-KP4 PMA/PMD. 0101101: 100GBASE-KR4 PMA/PMD. 0101110: 100GBASE-CR4 PMA/PMD. 0101111: 100GBASE-SR4 PMA/PMD. 0110000: 2.5GBASE-T PMA. 0110001: 5GBASE-T PMA. 0110010: 10GPASS-XR-D PMA/PMD. 0110011: 10GPASS-XR-U PMA/PMD. 0110100: BASE-H PMA/PMD. 0110101: 25GBASE-LR PMA/PMD. 0110110: 25GBASE-ER PMA/PMD. 0110111: 25GBASE-T PMA. 0111000: 25GBASE-CR or 25GBASE-CR-S PMA/PMD. 0111001: 25GBASE-KR or 25GBASE-KR-S PMA/PMD. 0111010: 25GBASE-SR PMA/PMD. 0111101: BASE-T1 PMA/PMD. 1010011: 200GBASE-DR4 PMA/PMD. 1010100: 200GBASE-FR4 PMA/PMD. 1010101: 200GBASE-LR4 PMA/PMD. 1011001: 400GBASE-SR16 PMA/PMD.		

REGISTER SUMMARY

Table 53. Bit Descriptions for PMA_PMD_CNTRL2 (Continued)

Bits	Bit Name	Description	Reset	Access
		1011010: 400GBASE-DR4 PMA/PMD. 1011011: 400GBASE-FR8 PMA/PMD. 1011100: 400GBASE-LR8 PMA/PMD.		

PMA/PMD Status 2 Register

Device Address: 0x01; Register Address: 0x0008, Reset: 0x8301, Name: PMA_PMD_STAT2

Table 54. Bit Descriptions for PMA_PMD_STAT2

Bits	Bit Name	Description	Reset	Access
[15:14]	PMA_PMD_PRESENT	PMA/PMD Present. Indicates that the PMA is present and responding.	0x2	R
[13:10]	RESERVED	Reserved.	0x0	R
9	PMA_PMD_EXT_ABLE	PHY Extended Abilities Support. Indicates that the PHY supports extended abilities as listed in PMA_PMD_EXT_ABILITY.	0x1	R
8	PMA_PMD_TX_DIS_ABLE	PMA/PMD Tx Disable. Indicates that the PMA supports transmit disable.	0x1	R
[7:1]	RESERVED	Reserved.	0x0	R
0	LB_PMA_LOC_ABLE	PMA Local Loopback Able. Indicates that the PMA supports local loopback.	0x1	R

PMA/PMD Transmit Disable Register

Device Address: 0x01; Register Address: 0x0009, Reset: 0x0000, Name: PMA_PMD_TX_DIS

This address corresponds to the PMD transmit disable register specified in Clause 45.2.1.8 of Standard 802.3.

Table 55. Bit Descriptions for PMA_PMD_TX_DIS

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	PMA_TX_DIS	PMD Transmit Disable. When this bit is set to 1, the PMD disables the output on the transmit path. Otherwise, the PMD enables the output on the transmit path.	0x0	R/W

PMA/PMD Extended Abilities Register

Device Address: 0x01; Register Address: 0x000B, Reset: 0x0800, Name: PMA_PMD_EXT_ABILITY

PMA/PMD extended abilities.

Table 56. Bit Descriptions for PMA_PMD_EXT_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	PMA_PMD_BT1_ABLE	PHY Supports BASE-T1. Indicates that the PHY supports BASE-T1 extended abilities as listed in PMA_PMD_BT1_ABILITY.	0x1	R
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 PMA/PMD Extended Ability Register

Device Address: 0x01; Register Address: 0x0012, Reset: 0x0004, Name: PMA_PMD_BT1_ABILITY

This address corresponds to the BASE-T1 PMA/PMD extended ability register specified in Clause 45.2.1.16 of Standard 802.3. This register is read only, and writes have no effect.

REGISTER SUMMARY

Table 57. Bit Descriptions for PMA_PMD_BT1_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	B10S_ABILITY	10BASE-T1S Ability. This bit always reads as 0 because the PMA/PMD does not support 10BASE-T1S.	0x0	R
2	B10L_ABILITY	10BASE-T1L Ability. This bit always reads as 1 because the PMA/PMD supports 10BASE-T1L.	0x1	R
1	B1000_ABILITY	1000BASE-T1 Ability. This bit always reads as 0 because the PMA/PMD does not support 1000BASE-T1.	0x0	R
0	B100_ABILITY	100BASE-T1 Ability. This bit always reads as 0 because the PMA/PMD does not support 100BASE-T1.	0x0	R

BASE-T1 PMA/PMD Control Register

Device Address: 0x01; Register Address: 0x0834, Reset: 0x8002, Name: PMA_PMD_BT1_CONTROL

This address corresponds to the BASE-T1 PMA/PMD control register specified in Clause 45.2.1.185 of Standard 802.3.

Table 58. Bit Descriptions for PMA_PMD_BT1_CONTROL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x1	R
14	CFG_MST	Leader and Follower Configuration. CFG_MST is used only when autonegotiation is disabled. Otherwise, this value is determined by the autonegotiation process itself. When this bit is set as 1, the device is configured as a leader. Otherwise, the device is configured as a follower.	Pin dependent	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	BT1_TYPE_SEL	BASE-T1 Type Selection. See IEEE Standard 802.3 for the following control register bit definitions (where X means don't care): 1XXX: reserved. 01XX: reserved. 0011: 10BASE-T1S . 0010: 10BASE-T1L. 0001: 1000BASE-T. 0000: 100BASE-T. BT1_TYPE_SEL is used only when autonegotiation is disabled and forced link configuration mode is enabled. If autonegotiation is enabled, the PHY type is determined by the autonegotiation process itself. Note that for ADIN1100, the only valid value is for 10BASE-T1L. 0010: 10BASE-T1L.	0x2	R/W

10BASE-T1L PMA Control Register

Device Address: 0x01; Register Address: 0x08F6, Reset: 0x0000, Name: B10L_PMA_CNTRL

This address corresponds to the 10BASE-T1L PMA control register specified in Clause 45.2.1.186a of Standard 802.3cg.

Table 59. Bit Descriptions for B10L_PMA_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_TX_DIS_MODE_EN	10BASE-T1L Transmit Disable Mode. When this bit is set to 1, it disables output on the transmit path. Otherwise, it enables output on the transmit path.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
12	B10L_TX_LVL_HI	10BASE-T1L Transmit Voltage Amplitude Control. This configuration is only used when autonegotiation is disabled. Otherwise, the configuration is decided by the autonegotiation process. When this bit is set as 1, the device works in the 2.4 V p-p operating mode. Otherwise, the device works in the 1.0 V p-p operating mode.	Pin dependent	R/W
11	RESERVED	Reserved.	0x0	R/W
10	B10L_EEE	10BASE-T1L EEE Enable.	0x0	R/W

REGISTER SUMMARY

Table 59. Bit Descriptions for B10L_PMA_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
[9:1]	RESERVED	Reserved.	0x0	R
0	B10L_LB_PMA_LOC_EN	10BASE-T1L PMA Loopback. When this bit is set to 1, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PMA works in normal mode.	0x0	R/W

10BASE-T1L PMA Status Register

Device Address: 0x01; Register Address: 0x08F7, Reset: 0x2800, Name: B10L_PMA_STAT

This address corresponds to the 10BASE-T1L PMA status register specified in Clause 45.2.1.186b of Standard 802.3cg.

Table 60. Bit Descriptions for B10L_PMA_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_LB_PMA_LOC_ABLE	10BASE-T1L PMA Loopback Ability. This bit always reads as 1 because the PMA has loopback ability.	0x1	R
12	B10L_TX_LVL_HI_ABLE	10BASE-T1L High Voltage Transmit Ability. Indicates that the PHY supports 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.	Pin dependent	R
11	B10L_PMA_SFT_PD_ABLE	PMA Supports Power-Down. Indicates that the PMA supports software power-down.	0x1	R
10	B10L_EEE_ABLE	10BASE-T1L EEE Ability. Indicates if the PHY supports 10BASE-T1L EEE.	0x0	R
[9:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L Test Mode Control Register

Device Address: 0x01; Register Address: 0x08F8, Reset: 0x0000, Name: B10L_TEST_MODE_CNTRL

This address corresponds to the 10BASE-T1L PMA test mode control register specified in Clause 45.2.1.186c of Standard 802.3cg. The default value of this register selects normal operation without management intervention as the initial state of the device.

Table 61. Bit Descriptions for B10L_TEST_MODE_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:13]	B10L_TX_TEST_MODE	10BASE-T1L Transmitter Test Mode. 000: normal operation. 001: Test Mode 1—transmitter output voltage and timing jitter test mode. When Test Mode 1 is enabled, the PHY repeatedly transmits the data symbol sequence (+1, −1). 010: Test Mode 2—transmitter output droop test mode. When Test Mode 2 is enabled, the PHY transmits ten +1 symbols followed by ten −1 symbols. 011: Test Mode 3—normal operation in idle mode. When Test Mode 3 is enabled, the PHY transmits as in nontest operation and in the leader data mode with data set to normal interframe idle signals.	0x0	R/W
[12:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PMA Link Status Register

Device Address: 0x01; Register Address: 0x8302, Reset: 0x0000, Name: B10L_PMA_LINK_STAT

This address can be read to determine the 10BASE-T1L PMA link status. Reading B10L_PMA_LINK_STAT clears the latching condition of the bits in Table 62.

Table 62. Bit Descriptions for B10L_PMA_LINK_STAT

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 62. Bit Descriptions for B10L_PMA_LINK_STAT (Continued)

Bits	Bit Name	Description	Reset	Access
9	B10L_REM_RCVR_STAT_OK_LL	10BASE-T1L Remote Receiver Status OK Latch Low. Latched low version of B10L_REM_RCVR_STAT_OK.	0x0	R LL
8	B10L_REM_RCVR_STAT_OK	10BASE-T1L Remote Receiver Status OK. When read as 1, this bit indicates that the remote receiver status is OK.	0x0	R
7	B10L_LOC_RCVR_STAT_OK_LL	10BASE-T1L Local Receiver Status OK Latch Low. Latched low version of B10L_LOC_RCVR_STAT_OK.	0x0	R LL
6	B10L_LOC_RCVR_STAT_OK	10BASE-T1L Local Receiver Status OK. When read as 1, this bit indicates that the local receiver status is OK.	0x0	R
5	B10L_DSCR_STAT_OK_LL	BASE-T1L Descrambler Status OK Latch Low. When read as 1, this bit indicates that the descrambler status is OK.	0x0	R LL
4	B10L_DSCR_STAT_OK	10BASE-T1L Descrambler Status OK. When read as 1, this bit indicates that the descrambler status is OK.	0x0	R
[3:2]	RESERVED	Reserved.	0x0	R
1	B10L_LINK_STAT_OK_LL	Link Status OK Latch Low. When read as 1, this bit indicates that the link status is OK.	0x0	R LL
0	B10L_LINK_STAT_OK	Link Status OK. When read as 1, this bit indicates that the link status is OK.	0x0	R

MSE Value Register

Device Address: 0x01; Register Address: 0x830B, Reset: 0x0000, Name: MSE_VAL

Table 63. Bit Descriptions for MSE_VAL

Bits	Bit Name	Description	Reset	Access
[15:0]	MSE_VAL	MSE Value. Note that the LSB weight is 2^{-18}. When computing a signal-to-noise ratio (SNR) value, the mean 10BASE-T1L idle symbol power is 0.64422.	0x0	R

PCS Control 1 Register

Device Address: 0x03; Register Address: 0x0000, Reset: 0x0000, Name: PCS_CNTRL1

This address corresponds to PCS Control Register 1 specified in Clause 45.2.3.1 of Standard 802.3.

Table 64. Bit Descriptions for PCS_CNTRL1

Bits	Bit Name	Description	Reset	Access
15	PCS_SFT_RST	PCS Software Reset. Mirrors PMA_SFT_RST.	0x0	R/W SC
14	LB_PCS_EN	PCS Loopback Enable. When this bit is set to 1, the PCS accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PCS works in normal mode.	0x0	R/W
[13:12]	RESERVED	Reserved.	0x0	R
11	PCS_SFT_PD	PCS Software Power-Down. Mirrors PMA_SFT_PD.	0x0	R/W
[10:0]	RESERVED	Reserved.	0x0	R

PCS Status 1 Register

Device Address: 0x03; Register Address: 0x0001, Reset: 0x0002, Name: PCS_STAT1

Table 65. Bit Descriptions for PCS_STAT1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	PCS_SFT_PD_ABLE	PCS Software Power-Down Able. Indicates that the PCS supports software power-down.	0x1	R
0	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

PCS MMD Devices in Package 1 Register

Device Address: 0x03; Register Address: 0x0005, Reset: 0x008B, Name: PCS_DEVS_IN_PKG1

Table 66. Bit Descriptions for PCS_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	PCS_DEVS_IN_PKG1	PCS MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

PCS MMD Devices in Package 2 Register

Device Address: 0x03; Register Address: 0x0006, Reset: 0xC000, Name: PCS_DEVS_IN_PKG2

Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.

Table 67. Bit Descriptions for PCS_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	PCS_DEVS_IN_PKG2	PCS MMD Devices in Package. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

PCS Status 2 Register

Device Address: 0x03; Register Address: 0x0008, Reset: 0x8000, Name: PCS_STAT2

Table 68. Bit Descriptions for PCS_STAT2

Bits	Bit Name	Description	Reset	Access
[15:14]	PCS_PRESENT	PCS Present. Indicates that the PCS is present and responding.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PCS Control Register

Device Address: 0x03; Register Address: 0x08E6, Reset: 0x0000, Name: B10L_PCS_CNTRL

This address corresponds to the 10BASE-T1L PCS control register specified in Clause 45.2.3.68a of Standard 802.3cg.

Table 69. Bit Descriptions for B10L_PCS_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_LB_PCS_EN	PCS Loopback Enable. When set to 1, this bit enables the 10BASE-T1L PCS loopback.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PCS Status Register

Device Address: 0x03; Register Address: 0x08E7, Reset: 0x0000, Name: B10L_PCS_STAT

This address corresponds to the 10BASE-T1L PCS status register specified in Clause 45.2.3.68b of Standard 802.3cg.

Table 70. Bit Descriptions for B10L_PCS_STAT

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	B10L_PCS_DSCR_STAT_OK_LL	PCS Descrambler Status. When read as 1, this bit indicates that the 10BASE-T1L descrambler is locked. When read as 0, this bit indicates that the 10BASE-T1L descrambler has unlocked since the last time the bit was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Autonegotiation MMD Devices in Package 1 Register

Device Address: 0x07; Register Address: 0x0005, Reset: 0x008B, Name: AN_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 71. Bit Descriptions for AN_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_DEVS_IN_PKG1	Autonegotiation MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Autonegotiation MMD Devices in Package 2 Register

Device Address: 0x07; Register Address: 0x0006, Reset: 0xC000, Name: AN_DEVS_IN_PKG2

Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.

Table 72. Bit Descriptions for AN_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_DEVS_IN_PKG2	Autonegotiation MMD Devices in Package 2. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x0200, Reset: 0x1000, Name: AN_CONTROL

This address corresponds to the BASE-T1 autonegotiation control register specified in Clause 45.2.7.19 of Standard 802.3.

Table 73. Bit Descriptions for AN_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R/W SC
12	AN_EN	Autonegotiation Enable. When this bit is set to 1, the autonegotiation is enabled. Autonegotiation is enabled by default and it is strongly recommended to always keep it enabled.	0x1	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	AN_RESTART	Autonegotiation Restart. Setting this bit to 1 restarts the autonegotiation process. This bit is self clearing, and it returns a value of 1 until the autonegotiation process is initiated.	0x0	R/W SC
[8:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x0201, Reset: 0x0008, Name: AN_STATUS

This address corresponds to the BASE-T1 autonegotiation status register specified in Clause 45.2.7.20 of Standard 802.3.

Table 74. Bit Descriptions for AN_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AN_PAGE_RX	Page Received. This bit is set to indicate that a new link codeword has been received and stored in the AN_LP_ADV_ABILITY_x register or the AN_LP_NEXT_PAGE_x register. The contents of AN_LP_ADV_ABILITY_x are valid when this bit is set the first time during autonegotiation. This bit resets to 0 on a read of the AN_STATUS register.	0x0	R LH
5	AN_COMPLETE	Autonegotiation Complete. When this bit is read as 1, it means that the autonegotiation process is complete, the PHY link is up, and that the contents of the AN_ADV_ABILITY_x and	0x0	R

REGISTER SUMMARY

Table 74. Bit Descriptions for AN_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
		AN_LP_ADV_ABILITY_x registers are valid. This bit returns 0 if the autonegotiation is disabled, clearing the AN_EN bit.		
4	AN_REMOTE_FAULT	Autonegotiation Remote Fault. Remote fault is set in the base page received from the link partner.	0x0	R LH
3	AN_ABLE	Autonegotiation Ability. When this bit is read as 1, it indicates that the PHY is able to perform autonegotiation.	0x1	R
2	AN_LINK_STATUS	Link Status. When read as 1, this bit indicates that a valid link has been established. If this bit reads 0, it means that the link has failed since the last time it was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0202, Reset: 0x0001, Name: AN_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits[15:0], specified in Clause 45.2.7.21 of Standard 802.3.

Table 75. Bit Descriptions for AN_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_ADV_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R/W
14	AN_ADV_ACK	Acknowledge (ACK). This bit indicates that the device has received the link codeword of its link partner. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_ADV_REMOTE_FAULT	Remote Fault. See IEEE Standard 802.3 Subclause 98.2.1.2.7.	0x0	R/W
12	AN_ADV_FORCE_MS	Force Leader/Follower Configuration. This bit allows the PHY to force its leader/follower configuration. When this bit is set as 0, the leader/follower configuration is a preferred mode. (The configuration in AN_ADV_MST is a preferred configuration.) If this bit is set to 1, the leader/follower configuration is a forced mode. (The configuration in AN_ADV_MST is a forced configuration.) See IEEE Standard 802.3 Subclause 98.2.1.2.5 for more details.	0x0	R/W
[11:10]	AN_ADV_PAUSE	Pause Ability. This bit field advertises support for asymmetric and symmetric pause functions on full duplex links. See IEEE Standard 802.3 Subclause 98.2.1.2.6 for more details.	0x0	R/W
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_ADV_SELECTOR	Selector. The value of this bit field is fixed at 00001, which is the IEEE 802.3 selector value. See IEEE Standard 802.3 Subclause 98.2.1.2.1.	0x1	R

BASE-T1 Autonegotiation Advertisement Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0203, Reset: 0x4000, Name: AN_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits[31:16], specified in Clause 45.2.7.21 of Standard 802.3.

Table 76. Bit Descriptions for AN_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_ADV_B10L	10BASE-T1L Ability. This bit indicates that the device is compatible with 10BASE-T1L.	0x1	R/W
[13:5]	RESERVED	Reserved.	0x0	R
4	AN_ADV_MST	Leader/Follower Configuration. This bit advertises the leader/follower configuration, as follows: 0: follower, 1: leader. See also the AN_ADV_FORCE_MS bit, which determines whether this bit expresses a preference or a forced value. See IEEE Standard 802.3 Subclause 98.2.1.2.3 (leader/follower configuration is Bit 4 of the transmitted nonce field).	Pin dependent	R/W
[3:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

BASE-T1 Autonegotiation Advertisement Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x0204, Reset: 0x0000, Name: AN_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits[47:32], specified in Clause 45.2.7.21 of Standard 802.3.

Table 77. Bit Descriptions for AN_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	AN_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This bit advertises that the PHY is capable of transmitting in the high level (2.4 V p-p) transmit operating mode. This bit is used with AN_ADV_B10L_TX_LVL_HI_REQ to configure the 10BASE-T1L transmission level (2.4 V p-p or 1.0 V p-p). See the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	Pin dependent	R/W
12	AN_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This bit advertises that the PHY is requesting that high level (2.4 V p-p) transmit operating mode be used. The transmit level is resolved as follows: If either PHY is not capable of high level transmission (and has AN_ADV_B10L_TX_LVL_HI_ABL = 0), both PHYs must use the low voltage (1.0 V p-p) transmit operating mode. Otherwise, if either PHY requests high level transmission (and has AN_ADV_B10L_TX_LVL_HI_REQ = 1), both PHYs must use the high voltage (2.4 V p-p) transmit operating mode. See IEEE P802.cg Subclause 146.6.4 for more details.	Pin dependent	R/W
[11:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0205, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[15:0], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of the AN_LP_ADV_ABILITY_M and AN_LP_ADV_ABILITY_H registers is latched when AN_LP_ADV_ABILITY_L is read.

Table 78. Bit Descriptions for AN_LP_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_ADV_NEXT_PAGE_REQ	Link Partner Next Page Request. This bit indicates that the link partner PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R
14	AN_LP_ADV_ACK	Link Partner Acknowledge (ACK). This bit indicates that the device has received the link codeword of its link partner. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_LP_ADV_REMOTE_FAULT	Link Partner Remote Fault. See IEEE Standard 802.3 Subclause 98.2.1.2.7.	0x0	R
12	AN_LP_ADV_FORCE_MS	Link Partner Force Leader/Follower Configuration. This bit reports the forced leader/follower configuration of the link partner, with values as follows. See IEEE Standard 802.3 Subclause 98.2.1.2.5 for more details. 0: preferred mode (AN_LP_ADV_MST is a preferred configuration). 1: forced mode (AN_LP_ADV_MST is a forced configuration).	0x0	R
[11:10]	AN_LP_ADV_PAUSE	Link Partner Pause Ability. This bit field reports the support of the link partner for asymmetric and symmetric pause functions on full duplex links. See IEEE Standard 802.3 Subclause 98.2.1.2.6 for more details.	0x0	R
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_LP_ADV_SELECTOR	Link Partner Selector. The value of this field reads 00001, which is the IEEE 802.3 selector value. See IEEE Standard 802.3 Subclause 98.2.1.2.1.	0x0	R

REGISTER SUMMARY

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0206, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[31:16], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 79. Bit Descriptions for AN_LP_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L	Link Partner 10BASE-T1L Ability. This bit indicates if the link partner has 10BASE-T1L ability.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
7	AN_LP_ADV_B1000	Link Partner 1000BASE-T1 Ability. This bit indicates if the link partner has 1000BASE-T1 ability.	0x0	R
6	AN_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This bit indicates if the link partner has 10BASE-T1S ability.	0x0	R
5	AN_LP_ADV_B100	Link Partner 100BASE-T1 Ability. This bit indicates if the link partner has 100BASE-T1 ability.	0x0	R
4	AN_LP_ADV_MST	Link Partner Leader/Follower Configuration. This bit reports the leader/follower configuration of the link partner, as follows: 0: follower, 1: leader. See also the AN_LP_ADV_FORCE_MS bit, which determines whether this bit expresses a preference or a forced value. See IEEE Standard 802.3 Subclause 98.2.1.2.3 (leader/follower configuration is Bit 4 of the transmitted nonce field).	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x0207, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[47:32], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 80. Bit Descriptions for AN_LP_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L_EEE	Link Partner 10BASE-T1L EEE Ability. This bit reports if the link partner is capable of using 10BASE-T1L energy efficient Ethernet.	0x0	R
13	AN_LP_ADV_B10L_TX_LVL_HI_ABL	Link Partner 10BASE-T1L High Level Transmit Operating Mode Ability. This bit reports whether the link partner is capable of transmitting in the high level (2.4 V p-p) transmit operating mode. This bit is used with AN_LP_ADV_B10L_TX_LVL_HI_REQ to configure the 10BASE-T1L transmission level (2.4 V p-p or 1.0 V p-p); see the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	0x0	R
12	AN_LP_ADV_B10L_TX_LVL_HI_REQ	Link Partner 10BASE-T1L High Level Transmit Operating Mode Request. This bit reports whether the link partner is requesting that the high level (2.4 V p-p) transmit operating mode be used. See the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	0x0	R
11	AN_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half-Duplex Ability. This bit reports if the link partner is capable of using 10BASE-T1S half duplex.	0x0	R
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0208, Reset: 0x2001, Name: AN_NEXT_PAGE_L

REGISTER SUMMARY

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[15:0], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 81. Bit Descriptions for AN_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R/W
14	AN_NP_ACK	Next Page Acknowledge. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_NP_MESSAGE_PAGE	Next Page Encoding. Indicates encoding of next page, as follows: 0: unformatted next page. 1: message next page.	0x1	R/W
12	AN_NP_ACK2	Acknowledge 2. Indicates whether the PHY can comply with the message. See IEEE Standard 802.3 Subclause 28.2.3.4.6.	0x0	R/W
11	AN_NP_TOGGLE	Toggle Bit. The toggle bit is used to synchronize pages between the PHYs. This always read as 0 (the toggle bit is set automatically by the arbitration state machine).	0x0	R
[10:0]	AN_NP_MESSAGE_CODE	Message/Unformatted Code Field. For a message page (AN_NP_MESSAGE_PAGE = 1), the valid values are defined in IEEE Standard 802.3. 1: null message. 5: organizationally unique identifier tagged message. 6: autonegotiation device identifier tag code.	0x1	R/W

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0209, Reset: 0x0000, Name: AN_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[31:16], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 82. Bit Descriptions for AN_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED1	Unformatted Code Field 1.	0x0	R/W

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x020A, Reset: 0x0000, Name: AN_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[47:42], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 83. Bit Descriptions for AN_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED2	Unformatted Code Field 2.	0x0	R/W

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x020B, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation next page ability register, Bits[15:0], of the link partner specified in Clause 45.2.7.24 of Standard 802.3. The values of AN_LP_NEXT_PAGE_M and AN_LP_NEXT_PAGE_H are latched when this register is read.

REGISTER SUMMARY

Table 84. Bit Descriptions for AN_LP_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R
14	AN_LP_NP_ACK	Link Partner Next Page Acknowledge. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_LP_NP_MESSAGE_PAGE	Link Partner Next Page Encoding. Indicates encoding of link partner next page, as follows: 0: unformatted next page. 1: message next page.	0x0	R
12	AN_LP_NP_ACK2	Link Partner Acknowledge 2. See AN_NP_ACK2 for more details.	0x0	R
11	AN_LP_NP_TOGGLE	Link Partner Toggle Bit. Link partner toggle bit.	0x0	R
[10:0]	AN_LP_NP_MESSAGE_CODE	Link Partner Message/Unformatted Code Field. See AN_NP_MESSAGE_PAGE for more details. 1: null message. 5: organizationally unique identifier tagged message. 6: autonegotiation device identifier tag code.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x020C, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page ability register, Bits[31:16], of the link partner specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 85. Bit Descriptions for AN_LP_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED1	Link Partner Unformatted Code Field 1.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x020D, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register, Bits[47:32], specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 86. Bit Descriptions for AN_LP_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED2	Link Partner Unformatted Code Field 2.	0x0	R

10BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x020E, Reset: 0x8000, Name: AN_B10_ADV_ABILITY

This address corresponds to the 10BASE-T1 autonegotiation control register specified in Clause 45.2.7.25 of Standard 802.3cg.

Table 87. Bit Descriptions for AN_B10_ADV_ABILITY

Bits	Bit Name	Description	Reset	Access
15	AN_B10_ADV_B10L	10BASE-T1L Ability. This bit is a duplicate of the AN_ADV_B10L bit.	0x1	R/W
14	AN_B10_ADV_B10L_EEE	10BASE-T1L EEE Ability. This bit is always read as 0, because the device does not have the energy efficient Ethernet ability.	0x0	R
13	AN_B10_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This is a duplicate of the AN_ADV_B10L_TX_LVL_HI_ABL bit.	Pin dependent	R/W

REGISTER SUMMARY

Table 87. Bit Descriptions for AN_B10_ADV_ABILITY (Continued)

Bits	Bit Name	Description	Reset	Access
12	AN_B10_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This is a duplicate of the AN_ADV_B10L_TX_LVL_HI_REQ bit.	Pin dependent	R/W
[11:0]	RESERVED	Reserved.	0x0	R

10BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x020F, Reset: 0x0000, Name: AN_B10_LP_ADV_ABILITY

This address corresponds to the 10BASE-T1 autonegotiation status register specified in Clause 45.2.7.26 of Standard 802.3cg.

Table 88. Bit Descriptions for AN_B10_LP_ADV_ABILITY

Bits	Bit Name	Description	Reset	Access
15	AN_B10_LP_ADV_B10L	10BASE-T1L Ability. This is a duplicate of the AN_LP_ADV_B10L bit.	0x0	R
14	AN_B10_LP_ADV_B10L_EEE	10BASE-T1L EEE Ability. This is a duplicate of the AN_LP_ADV_B10L_EEE bit.	0x0	R
13	AN_B10_LP_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This is a duplicate of the AN_LP_ADV_B10L_TX_LVL_HI_ABL bit.	0x0	R
12	AN_B10_LP_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This is a duplicate of the AN_LP_ADV_B10L_TX_LVL_HI_REQ bit.	0x0	R
[11:8]	RESERVED	Reserved.	0x0	R
7	AN_B10_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This is a duplicate of the AN_LP_ADV_B10S_FD bit.	0x0	R
6	AN_B10_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half-Duplex Ability. This is a duplicate of the AN_LP_ADV_B10S_HD bit.	0x0	R
[5:0]	RESERVED	Reserved.	0x0	R

Autonegotiation Forced Mode Enable Register

Device Address: 0x07; Register Address: 0x8000, Reset: 0x0000, Name: AN_FRC_MODE_EN

The effect of this register is superseded by the AN_EN bit, which enables the autonegotiation process. If autonegotiation is disabled (AN_EN = 0) and AN_FRC_MODE_EN = 1, forced mode is enabled.

Table 89. Bit Descriptions for AN_FRC_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	AN_FRC_MODE_EN	Autonegotiation Forced Mode. Enables forced mode functionality.	0x0	R/W

Extra Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x8001, Reset: 0x0000, Name: AN_STATUS_EXTRA

This register is provided in addition to AN_STATUS.

Table 90. Bit Descriptions for AN_STATUS_EXTRA

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	AN_LP_NP_RX	Next Page Request Received from Link Partner.	0x0	R LH
9	AN_INC_LINK	Incompatible Link Indication. This corresponds to the incompatible link state of IEEE Standard 802.3 Subclause 98.5.1. Its value is set by the priority resolution function run on entering the autonegotiation good check state.	0x0	R

REGISTER SUMMARY

Table 90. Bit Descriptions for AN_STATUS_EXTRA (Continued)

Bits	Bit Name	Description	Reset	Access
[8:7]	AN_TX_LVL_RSLTN	Autonegotiation Tx Level Result. Transmit level high/low resolution result, determined as per IEEE Standard 802.3cg Subclause 146.6.4. This is encoded as follows: 0: not run. 2: success, low transmit levels (1.0 V p-p) selected. 3: success, high transmit levels (2.4 V p-p) selected.	0x0	R
[6:5]	AN_MS_CONFIG_RSLTN	Leader/Follower Resolution Result. Determined as per leader/follower configuration of IEEE Standard 802.3. This is encoded as follows: 0: not run. 1: configuration fault. 2: success, PHY is configured as follower. 3: success, PHY is configured as leader.	0x0	R
[4:1]	AN_HCD_TECH	Highest Common Denominator (HCD) PHY Technology. As selected by the priority resolution function of IEEE Standard 802.3 Subclause 98.2.4.2. Consider all values that are not shown to be reserved. 0: null (not run). 1: 10BASE-T1L.	0x0	R
0	AN_LINK_GOOD	Autonegotiation Complete Indication. This corresponds to the an_link_good state of IEEE Standard 802.3 Subclause 98.5.1. This signal indicates completion of the autonegotiation transmission, and that the enabled PHY technology is either bringing up its link or that it has brought up its link. See also AN_COMPLETE, which is similar, but also indicates that the PHY link is up.	0x0	R

PHY Instantaneous Status Register

Device Address: 0x07; Register Address: 0x8030, Reset: 0x0010, Name: AN_PHY_INST_STATUS

This register address provides access to instantaneous status indications. These values are not latched. The set of indications returned by this register is a consistent set, that is, a set of values in effect at the time the register address is read.

Table 91. Bit Descriptions for AN_PHY_INST_STATUS

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
4	IS_AN_TX_EN	Autonegotiation Tx Enable Status. Autonegotiation transmit enable. This bit indicates that the autonegotiation is active and controlling the transmitter, and arbitration has not yet reached the autonegotiation (AN) good check state or the AN good state. That is, the link_control signals have not been set to enable.	0x1	R
3	IS_CFG_MST	Leader Status. If link_control = enable (for example, B10L_LINK_CTRL_EN = 1), this indicates whether the PHY is operating as leader (and not follower).	0x0	R
2	IS_CFG_SLV	Follower Status. If link_control = enable (for example, B10L_LINK_CTRL_EN = 1), this indicates whether the PHY is operating as follower (and not leader).	0x0	R
1	IS_TX_LVL_HI	Tx Level High Status. Indicates that the PHY is operating with high transmit levels (2.4 V), and not low transmit levels (1.0 V).	0x0	R
0	IS_TX_LVL_LO	Tx Level Low Status. Indicates that the PHY is operating with low transmit levels (1.0 V), and not low transmit levels (2.4 V).	0x0	R

Vendor Specific 1 MMD Identifier High Register

Device Address: 0x1E; Register Address: 0x0002, Reset: 0x0283, Name: MMD1_DEV_ID1

This address corresponds to the Vendor Specific 1 MMD identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

REGISTER SUMMARY

Table 92. Bit Descriptions for MMD1_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEV_ID1	Organizationally Unique Identifier, Bits[3:18].	0x283	R

Vendor Specific 1 MMD Identifier Low Register

Device Address: 0x1E; Register Address: 0x0003, Reset: 0xBC81, Name: MMD1_DEV_ID2

This address corresponds to the Vendor Specific 1 MMD identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows six bits of the OUI along with the model number and revision number to be observed.

Table 93. Bit Descriptions for MMD1_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD1_DEV_ID2_OUI	Organizationally Unique Identifier, Bits[19:24].	0x2F	R
[9:4]	MMD1_MODEL_NUM	Model Number.	0x8	R
[3:0]	MMD1_REV_NUM	Revision Number.	0x1	R

Vendor Specific 1 MMDs in Package Register

Device Address: 0x1E; Register Address: 0x0005, Reset: 0x008B, Name: MMD1_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 94. Bit Descriptions for MMD1_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEVS_IN_PKG1	Vendor Specific 1 MMDs in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Device Address: 0x1E; Register Address: 0x0006, Reset: 0xC000, Name: MMD1_DEVS_IN_PKG2

Vendor Specific 1 and Vendor Specific 2 MMDs are present.

Table 95. Bit Descriptions for MMD1_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEVS_IN_PKG2	Vendor Specific 1 MMDs in Package 2. Vendor Specific 1 and Vendor Specific 2 MMDs are present.	0xC000	R

Vendor Specific 1 MMD Status Register

Device Address: 0x1E; Register Address: 0x0008, Reset: 0x8000, Name: MMD1_STATUS

This address corresponds to the Vendor Specific 1 MMD status register specified in Clause 45.2.11.2 of Standard 802.3.

Table 96. Bit Descriptions for MMD1_STATUS

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD1_STATUS	Vendor Specific 1 MMD Status. 10: device responding at this address. 11: no device responding at this address. 01: no device responding at this address. 00: no device responding at this address.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

System Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0010, Reset: 0x1000, Name: CRSM_IRQ_STATUS

This address can be used to check which interrupt requests have been triggered since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of CRSM_IRQ_STATUS go high even when the associated interrupts are not enabled. A reserved interrupt being triggered indicates a system error, which requires a hardware reset.

Table 97. Bit Descriptions for CRSM_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_LH	Software Requested Interrupt Event.	0x0	R LH
[14:13]	RESERVED	Reserved.	0x0	R
12	CRSM_HRD_RST_IRQ_LH	Hardware Reset Interrupt.	0x1	R LH
[11:0]	RESERVED	Reserved.	0x0	R LH

System Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0020, Reset: 0x1FFE, Name: CRSM_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 98. Bit Descriptions for CRSM_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_REQ	Software Interrupt Request. Software can set this bit to generate an interrupt for system level testing. This bit always reads as 0 because it is self clearing.	0x0	R/W SC
[14:13]	RESERVED	Reserved.	0x0	R
12	CRSM_HRD_RST_IRQ_EN	Enable Hardware Reset Interrupt. Note that writing a 0 to this bit does not mask the interrupt because this bit is initialized when a hardware reset occurs.	0x1	R/W
[11:0]	RESERVED	Reserved.	0xFFE	R/W

Software Reset Register

Device Address: 0x1E; Register Address: 0x8810, Reset: 0x0000, Name: CRSM_SFT_RST

Table 99. Bit Descriptions for CRSM_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_RST	Software Reset Register. The software reset bit allows the chip to be reset. When this bit is set, the chip fully initializes, almost equivalent to a hardware reset.	0x0	R/W SC

Software Power-Down Control Register

Device Address: 0x1E; Register Address: 0x8812, Reset: 0x0000, Name: CRSM_SFT_PD_CNTRL

Table 100. Bit Descriptions for CRSM_SFT_PD_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_PD	Software Power-Down. The software power-down register puts the chip in a lower power mode. In this mode, most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via the RX_DV/RX_CTL/$\overline{\text{SWPD\_EN}}$ pin. This pin allows the chip to be held in power-down mode until an appropriate software initialization is performed.	Pin dependent	R/W

REGISTER SUMMARY

PHY Subsystem Reset Register

Device Address: 0x1E; Register Address: 0x8814, Reset: 0x0000, Name: CRSM_PHY_SUBSYS_RST

Table 101. Bit Descriptions for CRSM_PHY_SUBSYS_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset. The PHY subsystem reset register allows a managed subsystem reset to be initiated. When the PHY subsystem is reset, normal operation resumes, and the bit self clears.	0x0	R/W SC

PHY MAC Interface Reset Register

Device Address: 0x1E; Register Address: 0x8815, Reset: 0x0000, Name: CRSM_MAC_IF_RST

Table 102. Bit Descriptions for CRSM_MAC_IF_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_MAC_IF_RST	PHY MAC Interface Reset. The PHY MAC interface reset register allows a managed PHY MAC interface reset to be initiated. When the PHY MAC interface is reset, normal operation resumes, and the bit self clears.	0x0	R/W SC

System Status Register

Device Address: 0x1E; Register Address: 0x8818, Reset: 0x0000, Name: CRSM_STAT

Table 103. Bit Descriptions for CRSM_STAT

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	CRSM_SFT_PD_RDY	Software Power-Down Status. This bit indicates that the system is in the software power-down state.	0x0	R
0	CRSM_SYS_RDY	System Ready. This bit indicates that the start-up sequence is complete and the system is ready for normal operation.	0x0	R

CRSM Power Management Control Register

Device Address: 0x1E; Register Address: 0x8819, Reset: 0x0000, Name: CRSM_PMG_CNTRL

Table 104. Bit Descriptions for CRSM_PMG_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_FRC_OSC_EN	Force Digital Boot Oscillator Clock Enable.	0x0	R/W

MAC Interface Configuration Register

Device Address: 0x1E; Register Address: 0x882B, Reset: 0x0000, Name: CRSM_MAC_IF_CFG

Configure the MAC interface only by pins. Do not change by software.

Table 105. Bit Descriptions for CRSM_MAC_IF_CFG

Bits	Bit Name	Description	Reset	Access
15	CRSM_RMII_CLK50	This Bit Indicates If the RMII REF_CLK Frequency is 50 MHz or 25 MHz. Only for debugging purposes.	Pin dependent	R/W
14	CRSM_RMII_CLK_EN	CRSM RMII Clock Enable Status. This bit indicates if the RMII clock generation is enabled.	Pin dependent	R/W

REGISTER SUMMARY

Table 105. Bit Descriptions for CRSM_MAC_IF_CFG (Continued)

Bits	Bit Name	Description	Reset	Access
[13:9]	RESERVED	Reserved.	0x0	R
8	CRSM_RMII_MEDIA_CNV_EN	Media Converter Enable. When this bit is 1, the media converter functionality for the RMII MAC interface mode is enabled. Note that the media converter functionality can only be enabled if an RMII MAC interface is being used.	Pin dependent	R/W
[7:5]	RESERVED	Reserved.	0x0	R
4	CRSM_RMII_EN	RMII MAC Interface Enable. Enable RMII MAC interface mode. Do not set CRSM_RGMII_EN and CRSM_RMII_EN at the same time. Configure the MAC interface only by pins. Do not change by software.	Pin dependent	R/W
[3:1]	RESERVED	Reserved.	0x0	R
0	CRSM_RGMII_EN	RGMII MAC Interface Enable. Enable RGMII MAC interface mode. Do not set CRSM_RGMII_EN and CRSM_RMII_EN at the same time. Configure the MAC interface only by pins. Do not change by software.	Pin dependent	R/W

CRSM Diagnostics Clock Control Register

Device Address: 0x1E; Register Address: 0x882C, Reset: 0x0002, Name: CRSM_DIAG_CLK_CTRL

CRSM diagnostics clock control.

Table 106. Bit Descriptions for CRSM_DIAG_CLK_CTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x1	R
0	CRSM_DIAG_CLK_EN	Enable the Diagnostics Clock.	0x0	R/W

Package Configuration Values Register

Device Address: 0x1E; Register Address: 0x8C22, Reset: 0x0002, Name: MGMT_PRT_PKG

The MGMT_PRT_PKG_VAL address allows reading of the package configuration values.

Table 107. Bit Descriptions for MGMT_PRT_PKG

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	MGMT_PRT_PKG_VAL	Package Type. 2 = ADIN1100 40-lead LFCSP.	0x2	R

MDIO Control Register

Device Address: 0x1E; Register Address: 0x8C30, Reset: 0x0000, Name: MGMT_MDIO_CNTRL

Table 108. Bit Descriptions for MGMT_MDIO_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	MGMT_GRP_MDIO_EN	Enable MDIO PHY/Port Group Address Mode. In this mode, the PHY responds to any write or address operation to the 5-bit PHY/Port Address 31 (decimal) regardless of its own PHY/port address. This feature is only intended for initialization sequences in multiport applications, must only be set in those cases, and cleared immediately after the initialization is complete.	0x0	R/W

REGISTER SUMMARY

Pin Mux Configuration 1 Register

Device Address: 0x1E; Register Address: 0x8C56, Reset: 0x00FE, Name: DIGIO_PINMUX

Table 109. Bit Descriptions for DIGIO_PINMUX

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0xF	R
[3:1]	DIGIO_LED1_PINMUX	Pin Mux Select for LED_1. 000: LED_1. 111: LED_1 output not enabled.	0x7	R/W
0	DIGIO_LINK_ST_POLARITY	LINK_ST Polarity. 0: assert high. 1: assert low.	0x0	R/W

Pin Mux Configuration 2 Register

Device Address: 0x1E; Register Address: 0x8C57, Reset: 0x00FF, Name: DIGIO_PINMUX2

Table 110. Bit Descriptions for DIGIO_PINMUX2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:4]	DIGIO_RXSOP_PINMUX	Pin Mux Select for Receive SOP. 0000: RXD_3. 0001: RXD_2. 0010: RXD_1. 0011: RX_CLK. 0100: RX_DV. 0101: RX_ER. 0110: TX_ER. 0111: TX_EN. 1000: TX_CLK. 1001: TXD_1. 1010: TXD_2. 1011: TXD_3. 1100: LINK_ST. 1101: LED_0. 1110: LED_1. 1111: off.	0xF	R/W
[3:0]	DIGIO_TXSOP_PINMUX	Pin Mux Select for Transmit SOP. 0000: RXD_3. 0001: RXD_2. 0010: RXD_1. 0011: RX_CLK. 0100: RX_DV. 0101: RX_ER. 0110: TX_ER. 0111: TX_EN. 1000: TX_CLK. 1001: TXD_1. 1010: TXD_2.	0xF	R/W

REGISTER SUMMARY

Table 110. Bit Descriptions for DIGIO_PINMUX2 (Continued)

Bits	Bit Name	Description	Reset	Access
		1011: TXD_3. 1100: LINK_ST. 1101: LED_0. 1110: LED_1. 1111: off.		

LED_0 On/Off Blink Time Register

Device Address: 0x1E; Register Address: 0x8C80, Reset: 0x3636, Name: LED0_BLINK_TIME_CNTRL

LED on blink time = LED0_ON_N4MS × 4 ms.

LED off blink time = LED0_OFF_N4MS × 4 ms.

If LEDx_MODE = 0 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED off sequence, followed by an LED on sequence, and then repeats.

If LEDx_MODE = 1 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED on sequence, followed by an LED off sequence, and then repeats.

If LEDx_OFF_N4MS = LEDx_ON_N4MS = 0, this is a special case whereby the internal activity signal as selected by LEDx_FUNCTION can be monitored live.

If LEDx_FUNCTION is programmed to a combination of a link and activity signal, the LED is on while the link is up and with no activity. The LED switches off for either loss of link or receipt of activity.

If LEDx_FUNCTION is programmed to an activity signal, the LED is off with no activity. The LED switches on upon receipt of activity.

Table 111. Bit Descriptions for LED0_BLINK_TIME_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	LED0_ON_N4MS	LED_0 On Blink Time. LED_0 on blink time is calculated by 4 ms × LED0_ON_N4MS bit field. Recommended value is greater than 3.	0x36	R/W
[7:0]	LED0_OFF_N4MS	LED_0 Off Blink Time. LED_0 off blink time is calculated by 4 ms × LED0_OFF_N4MS bit field. Recommended value is greater than 3.	0x36	R/W

LED_1 On/Off Blink Time Register

Device Address: 0x1E; Register Address: 0x8C81, Reset: 0x3636, Name: LED1_BLINK_TIME_CNTRL

LED on blink time = LED1_ON_N4MS × 4ms.

LED off blink time = LED1_OFF_N4MS × 4 ms.

If LEDx_MODE = 0 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED off sequence followed by an LED on sequence, and then repeats.

If LEDx_MODE = 1 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED on sequence, followed by an LED Off sequence, and then repeats.

If LEDx_OFF_N4MS = LEDx_ON_N4MS = 0, this is a special case whereby the internal activity signal as selected by LEDx_FUNCTION can be monitored live.

If LEDx_FUNCTION is programmed to a combination of a link and activity signal, the LED is on while the link is up and with no activity. The LED switches off for either loss of link or receipt of activity.

If LEDx_FUNCTION is programmed to an activity signal, the LED is off with no activity. The LED switches on upon receipt of activity.

REGISTER SUMMARY

Table 112. Bit Descriptions for LED1_BLINK_TIME_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	LED1_ON_N4MS	LED_1 On Blink Time. LED_1 on blink time is calculated by 4 ms × LED1_ON_N4MS bit field. Recommended value is greater than 3.	0x36	R/W
[7:0]	LED1_OFF_N4MS	LED_1 Off Blink Time. LED_1 off blink time is calculated by 4 ms × LED1_OFF_N4MS bit field. Recommended value is greater than 3.	0x36	R/W

LED Control Register

Device Address: 0x1E; Register Address: 0x8C82, Reset: 0x8480, Name: LED_CNTRL

LED control register

Table 113. Bit Descriptions for LED_CNTRL

Bits	Bit Name	Description	Reset	Access
15	LED1_EN	LED 1 Enable. A disabled LED is off. An enabled LED can be on or blinking depending on LED1_FUNCTION selection and activity.	0x1	R/W
14	LED1_LINK_ST_QUALIFY	Qualify Certain LED 1 Options with link_status. 0: TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower not qualified by link_status. 1: TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower are qualified by link_status.	0x0	R/W
13	LED1_MODE	LED 1 Mode Selection. 0: LED Mode 1. If there is activity, blink at the rate defined by MMR LED1_BLINK_TIME_CNTRL. 1: LED Mode 2. The LED blink frequency is set depending on the level of activity. The activity level is graded in steps of 10%, and the frequency of the LED adjusts accordingly. A higher activity level means a longer off duration and shorter on duration. The activity level is reevaluated after a window period that varies between 640 ms and 1.5 sec.	0x0	R/W
[12:8]	LED1_FUNCTION	LED_1 Pin Function. Determines the source activity for the LED_1 pin. The CLK25_REF, TX_TCLK, and CLK_120MHZ options are clock out features with the LED controller bypassed. The waveform transmitted off chip is dependent on the selected clock source frequency. The following LED1_FUNCTION settings are not qualified with link_status: LED1_FUNCTION = on, off, blink, INCOMPATIBLE_LINK_CFG, AN_LINK_GOOD, AN_COMPLETE, LOC_RCVR_STATUS, REM_RCVR_STATUS, CLK25_REF, TX_TCLK, and CLK_120MHz. The TX_LEVEL_2P4, TX_LEVEL_1P0, leader, and follower options are optionally qualified by link_status and this is controlled via the LED1_LINK_ST_QUALIFY MMR. The TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower, MSTR_SLV_FAULT, AN_LINK_GOOD, AN_COMPLETE, and TS_TIMER options are considered status indicators and the LED controller is not used. If the programmed signal is high, the LED is static on and if the programmed signal is low, the LED is static off. 0: LINKUP_TXRX_ACTIVITY. 1: LINKUP_TX_ACTIVITY. 2: LINKUP_RX_ACTIVITY. 3: LINKUP_ONLY. 4: TXRX_ACTIVITY. 5: TX_ACTIVITY. 6: RX_ACTIVITY. 7: LINKUP_RX_ER (available in LED Mode 1 only). 8: LINKUP_RX_TX_ER (available in LED Mode 1 only). 9: RX_ER (available in LED Mode 1 only). 10: RX_TX_ER (available in LED Mode 1 only). 11: TX_SOP. 12: RX_SOP. 13: on. 14: off.	0xE	R/W

REGISTER SUMMARY

Table 113. Bit Descriptions for LED_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
		15: blink. 16: TX_LEVEL_2P4. 17: TX_LEVEL_1P0. 18: leader. 19: follower. 20: INCOMPATIBLE_LINK_CFG. 21: AN_LINK_GOOD. 22: AN_COMPLETE. 23: TS_TIMER. 24: LOC_RCVR_STATUS. 25: REM_RCVR_STATUS. 26: CLK25_REF. 27: TX_TCLK. 28: CLK_120MHZ.		
7	LED0_EN	LED 0 Enable. A disabled LED is off. An enabled LED can be on or blinking depending on LED0_FUNCTION selection and activity.	0x1	R/W
6	LED0_LINK_ST_QUALIFY	Qualify Certain LED 0 Options with link_status. 0: TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower not qualified by link_status. 1: TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower are qualified by link_status.	0x0	R/W
5	LED0_MODE	LED 0 Mode Selection. 0: LED Mode 1. If activity, blink at the rate defined by MMR LED0_BLINK_TIME_CNTRL. 1: LED Mode 2. The LED blink frequency is set depending on the level of activity. The activity level is graded in steps of 10%, and the frequency of the LED adjusts accordingly. A higher activity level means a longer off duration and shorter on duration. The activity level is reevaluated after a window period that varies between 640 ms and 1.5 sec.	0x0	R/W
[4:0]	LED0_FUNCTION	LED_0 Pin Function. Determines the source activity for the LED_0 pin. The CLK25_REF, TX_TCLK, CLK_120MHZ options are clock out features with the LED controller bypassed. The waveform transmitted off chip is dependent on the selected clock source frequency. The following LED_FUNCTION settings are not qualified with link_status: LED_FUNCTION = on, off, blink, INCOMPATIBLE_LINK_CFG, AN_LINK_GOOD, AN_COMPLETE, LOC_RCVR_STATUS, REM_RCVR_STATUS, CLK25_REF, TX_TCLK and CLK_120MHz. Options TX_LEVEL_2P4, TX_LEVEL_1P0, leader, and follower are optionally qualified by link status and this is controlled via the LED0_LINK_ST_QUALIFY MMR. The TX_LEVEL_2P4, TX_LEVEL_1P0, leader, follower, MSTR_SLV_FAULT, AN_LINK_GOOD, AN_COMPLETE, and TS_TIMER. These options are considered status indicators and the LED controller is not used. If the programmed signal is high, the LED is static on and if the programmed signal is low, the LED is static off. 0: LINKUP_TXRX_ACTIVITY. 1: LINKUP_TX_ACTIVITY. 2: LINKUP_RX_ACTIVITY. 3: LINKUP_ONLY. 4: TXRX_ACTIVITY. 5: TX_ACTIVITY. 6: RX_ACTIVITY. 7: LINKUP_RX_ER (available in LED Mode 1 only). 8: LINKUP_RX_TX_ER (available in LED Mode 1 only). 9: RX_ER (available in LED Mode 1 only). 10: RX_TX_ER (available in LED Mode 1 only). 11: TX_SOP. 12: RX_SOP.	0x0	R/W

REGISTER SUMMARY

Table 113. Bit Descriptions for LED_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
		13: on. 14: off. 15: blink. 16: TX_LEVEL_2P4. 17: TX_LEVEL_1P0. 18: leader. 19: follower. 20: INCOMPATIBLE_LINK_CFG. 21: AN_LINK_GOOD. 22: AN_COMPLETE. 23: TS_TIMER. 24: LOC_RCVR_STATUS. 25: REM_RCVR_STATUS. 26: CLK25_REF. 27: TX_TCLK. 28: CLK_120MHZ.		

LED Polarity Register

Device Address: 0x1E; Register Address: 0x8C83, Reset: 0x0000, Name: LED_POLARITY

Allows the LED polarity to be automatically sensed by the internal logic or allows reconfiguration by the user.

Table 114. Bit Descriptions for LED_POLARITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:2]	LED1_POLARITY	LED_1 Polarity. 0: LED autosense. LED active high or low as per autosense. 1: LED active high. 2: LED active low.	0x0	R/W
[1:0]	LED0_POLARITY	LED_0 Polarity. 0: LED autosense. LED active high or low as per autosense. 1: LED active high. 2: LED active low.	0x0	R/W

Vendor Specific MMD 2 Device Identifier High Register

Device Address: 0x1F; Register Address: 0x0002, Reset: 0x0283, Name: MMD2_DEV_ID1

Table 115. Bit Descriptions for MMD2_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEV_ID1	Vendor Specific MMD 2 Device Identifier.	0x283	R

Vendor Specific MMD 2 Device Identifier Low Register

Device Address: 0x1F; Register Address: 0x0003, Reset: 0xBC81, Name: MMD2_DEV_ID2

REGISTER SUMMARY

Table 116. Bit Descriptions for MMD2_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD2_DEV_ID2_OUI	OUI Bits.	0x2F	R
[9:4]	MMD2_MODEL_NUM	Model Number.	0x8	R
[3:0]	MMD2_REV_NUM	Revision Number.	0x1	R

Vendor Specific 2 MMDs in Package Register

Device Address: 0x1F; Register Address: 0x0005, Reset: 0x008B, Name: MMD2_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 117. Bit Descriptions for MMD2_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEVS_IN_PKG1	Vendor Specific 2 MMDs in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Device Address: 0x1F; Register Address: 0x0006, Reset: 0xC000, Name: MMD2_DEVS_IN_PKG2

Vendor Specific 1 and Vendor Specific 2 MMDs are present.

Table 118. Bit Descriptions for MMD2_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEVS_IN_PKG2	Vendor Specific 2 MMDs in Package 2. Vendor Specific 1 and Vendor Specific 2 MMDs are present.	0xC000	R

Vendor Specific MMD 2 Status Register

Device Address: 0x1F; Register Address: 0x0008, Reset: 0x8000, Name: MMD2_STATUS

This address corresponds to the Vendor Specific MMD 2 status register.

Table 119. Bit Descriptions for MMD2_STATUS

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD2_STATUS	Vendor Specific MMD 2 Status. 10: device responding at this address. 11: no device responding at this address. 01: no device responding at this address. 00: no device responding at this address.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

PHY Subsystem Interrupt Status Register

Device Address: 0x1F; Register Address: 0x0011, Reset: 0x0000, Name: PHY_SUBSYS_IRQ_STATUS

This address can be read to check which interrupt events have occurred since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of PHY_SUBSYS_IRQ_STATUS go high even when the associated bits in PHY_SUBSYS_IRQ_MASK are not set. A reserved interrupt being triggered indicates a fatal error in the system.

Table 120. Bit Descriptions for PHY_SUBSYS_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R LH
14	MAC_IF_FC_FG_IRQ_LH	MAC Interface Frame Checker/Generator Interrupt.	0x0	R LH
13	MAC_IF_EBUF_ERR_IRQ_LH	MAC Interface Buffers Overflow/Underflow Interrupt.	0x0	R LH

REGISTER SUMMARY

Table 120. Bit Descriptions for PHY_SUBSYS_IRQ_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
12	RESERVED	Reserved.	0x0	R LH
11	AN_STAT_CHNG_IRQ_LH	Autonegotiation Status Change Interrupt.	0x0	R LH
[10:2]	RESERVED	Reserved.	0x0	R LH
1	LINK_STAT_CHNG_LH	Link Status Change.	0x0	R LH
0	RESERVED	Reserved.	0x0	R LH

PHY Subsystem Interrupt Mask Register

Device Address: 0x1F; Register Address: 0x0021, Reset: 0x2402, Name: PHY_SUBSYS_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 121. Bit Descriptions for PHY_SUBSYS_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	MAC_IF_FC_FG_IRQ_EN	Enable MAC Interface Frame Checker/Generator Interrupt.	0x0	R/W
13	MAC_IF_EBUF_ERR_IRQ_EN	Enable MAC Interface Buffers Overflow/Underflow Interrupt.	0x1	R/W
12	RESERVED	Reserved.	0x0	R/W
11	AN_STAT_CHNG_IRQ_EN	Enable Autonegotiation Status Change Interrupt.	0x0	R/W
[10:2]	RESERVED	Reserved.	0x100	R/W
1	LINK_STAT_CHNG_IRQ_EN	Enable Link Status Change Interrupt.	0x1	R/W
0	RESERVED	Reserved.	0x0	R/W

Frame Checker Enable Register

Device Address: 0x1F; Register Address: 0x8001, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 122. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	Frame Checker Enable. Set to 1 to enable the frame checker.	0x1	R/W

Frame Checker Interrupt Enable Register

Device Address: 0x1F; Register Address: 0x8004, Reset: 0x0001, Name: FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register.

Table 123. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	Frame Checker Interrupt Enable. When set, this bit enables the frame checker interrupt.	0x1	R/W

REGISTER SUMMARY

Frame Checker Transmit Select Register

Device Address: 0x1F; Register Address: 0x8005, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received from the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (see the MAC_IF_REM_LB_EN bit in the MAC_IF_LOOPBACK register) because it can be used to check the received data after it is looped back at the MAC interface.

Table 124. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	Frame Checker Transmit Select. When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Receive Error Count Register

Device Address: 0x1F; Register Address: 0x8008, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY.

Table 125. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	Receive Error Count. This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self clearing upon reading.	0x0	R SC

Frame Checker Count High Register

Device Address: 0x1F; Register Address: 0x8009, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits[31:16] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and the receive frame count are synchronized.

Table 126. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits[31:16] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Count Low Register

Device Address: 0x1F; Register Address: 0x800A, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits[15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and receive frame count are synchronized.

Table 127. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits[15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Length Error Count Register

Device Address: 0x1F; Register Address: 0x800B, Reset: 0x0000, Name: FC_LEN_ERR_CNT

REGISTER SUMMARY

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized.

Table 128. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Alignment Error Count Register

Device Address: 0x1F; Register Address: 0x800C, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT) is read, the alignment error counter is latched, which ensures that the frame alignment error count and the receive frame count are synchronized.

Table 129. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Count Register

Device Address: 0x1F; Register Address: 0x800D, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT) is read, the symbol error count is latched, which ensures that the symbol error count and the frame receive count are synchronized.

Table 130. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYMB_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Oversized Frame Count Register

Device Address: 0x1F; Register Address: 0x800E, Reset: 0x0000, Name: FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of receiver frames with a length greater than 1522 bytes. When the receive error counter (RX_ERR_CNT) is read, the oversized frame counter register is latched, which ensures that the oversized error count and the receive frame count are synchronized.

Table 131. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched Copy of the Oversized Frame Error Counter.	0x0	R

Frame Checker Undersized Frame Count Register

Device Address: 0x1F; Register Address: 0x800F, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with less than 64 bytes. When the receive error counter (RX_ERR_CNT) is read, the undersized frame error counter is latched, which ensures that the undersized frame error count and the receive frame count are synchronized.

REGISTER SUMMARY

Table 132. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Device Address: 0x1F; Register Address: 0x8010, Reset: 0x0000, Name: FC_ODD_CNT

This register is a latched copy of the odd nibble frame register. This register is a count of received frames with an odd number of nibbles in the frame. When the receive error counter (RX_ERR_CNT) is read, the odd nibble frame counter register is latched, which ensures that the odd nibble frame count and the receive frame count are synchronized.

Table 133. Bit Descriptions for FC_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_CNT	Latched Copy of the Odd Nibble Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Device Address: 0x1F; Register Address: 0x8011, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received packets with an odd number of nibbles in the preamble. When the receive error counter (RX_ERR_CNT) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and the receive frame count are synchronized.

Table 134. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_PRE_CNT	Latched Copy of the Odd Preamble Packet Counter.	0x0	R

Frame Checker False Carrier Count Register

Device Address: 0x1F; Register Address: 0x8013, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This register is a count of the number of times the bad SSD state is entered. When the receive error counter (RX_ERR_CNT) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and the receive frame count are synchronized.

Table 135. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Device Address: 0x1F; Register Address: 0x8020, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface.

Table 136. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_EN	Frame Generator Enable.	0x0	R/W

REGISTER SUMMARY

Frame Generator Control/Restart Register

Device Address: 0x1F; Register Address: 0x8021, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register controls the frame generator. The FG_CNTRL bit field specifies data field type used by the frame generator, for example, random or all zeros. The FG_RSTRT bit restarts the frame generator.

Table 137. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	Frame Generator Restart. When set, this bit restarts the frame generator. This bit is self clearing.	0x0	R/W SC
[2:0]	FG_CNTRL	Frame Generator Control. 000: no frames after completion of current frame. 001: random number data frame. 010: all zeros data frame. 011: all ones data frame. 100: alternative 0x55 data field. 101: data field decrementing from 255 (decimal) to 0.	0x1	R/W

Frame Generator Continuous Mode Enable Register

Device Address: 0x1F; Register Address: 0x8022, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H and FG_NFRM_L registers.

Table 138. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable. This bit is used to put the frame generator into continuous mode or burst mode. 1: frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames is determined by the FG_NFRM_H and FG_NFRM_L registers.	0x0	R/W

Frame Generator Interrupt Enable Register

Device Address: 0x1F; Register Address: 0x8023, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The interrupt status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register.

Table 139. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	Frame Generator Interrupt Enable. When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

REGISTER SUMMARY

Frame Generator Frame Length Register

Device Address: 0x1F; Register Address: 0x8025, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the data field frame length in bytes. In addition to the data field, six bytes are added for the source address, six bytes for the destination address, two bytes for the length field, and four bytes for the frame check sequence (FCS). The total length is the data field length plus 18.

Table 140. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Interframe Gap Length Register

Device Address: 0x1F; Register Address: 0x8026, Reset: 0x000C, Name: FG_IFG_LEN

This register specifies the length in bytes of the interframe gap to be inserted between frames by the frame generator.

Table 141. Bit Descriptions for FG_IFG_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_IFG_LEN	Frame Generator Interframe Gap Length. This register specifies the length in bytes of the interframe gap to be inserted between frames by the frame generator.	0xC	R/W

Frame Generator Number of Frames High Register

Device Address: 0x1F; Register Address: 0x8027, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits[31:16] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 142. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits[31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Device Address: 0x1F; Register Address: 0x8028, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits[15:0] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 143. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits[15:0] of the Number of Frames to be Generated.	0x100	R/W

Frame Generator Done Register

Device Address: 0x1F; Register Address: 0x8029, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H and FG_NFRM_L registers.

REGISTER SUMMARY

Table 144. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	Frame Generator Done. This bit reads as 1 to indicate that the generation of frames has completed. When set, this bit goes high and it latches high until it is unlatched by reading.	0x0	R LH

RMII Configuration Register

Device Address: 0x1F; Register Address: 0x8050, Reset: 0x0006, Name: RMII_CFG

Table 145. Bit Descriptions for RMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x3	R
0	RMII_TXD_CHK_EN	RMII TXD Check Enable. This bit determines whether or not TXD_1 to TXD_0 are monitored to detect the start of a frame. It allows the RMII receiver CRS_DV signal to be connected to the RMII TX_EN signal. It is mainly intended for debug and test purposes.	0x0	R/W

MAC Interface Loopbacks Configuration Register

Device Address: 0x1F; Register Address: 0x8055, Reset: 0x000A, Name: MAC_IF_LOOPBACK

MAC interface loopbacks configuration.

Table 146. Bit Descriptions for MAC_IF_LOOPBACK

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	MAC_IF_REM_LB_RX_SUP_EN	Suppress RX Enable. Suppress receiver to the MAC when MAC_IF_REM_LB_EN is set.	0x1	R/W
2	MAC_IF_REM_LB_EN	MAC Interface Remote Loopback Enable. Receive data is looped back to the transmitter.	0x0	R/W
1	MAC_IF_LB_TX_SUP_EN	Suppress Transmission Enable. Suppress transmission to the PHY when MAC_IF_LB_EN is set.	0x1	R/W
0	MAC_IF_LB_EN	MAC Interface Loopback Enable. Transmit data is looped back to the receiver.	0x0	R/W

MAC Start of Packet (SOP) Generation Control Register

Device Address: 0x1F; Register Address: 0x805A, Reset: 0x001B, Name: MAC_IF_SOP_CNTRL

Table 147. Bit Descriptions for MAC_IF_SOP_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	MAC_IF_TX_SOP_LEN_CHK_EN	Enable TX SOP Preamble Length Check.	0x0	R/W
4	MAC_IF_TX_SOP_SFD_EN	Enable TX SOP Signal Indication on start of frame delimiter (SFD).	0x1	R/W
3	MAC_IF_TX_SOP_DET_EN	Enable the Generation of the TX SOP Indication Signal.	0x1	R/W
2	MAC_IF_RX_SOP_LEN_CHK_EN	Enable RX SOP Preamble Length Check. If this bit is set and no SFD is received, the RX SOP signal indication is set after eight bytes. Otherwise, the RX SOP is not set if no SFD is received in the first eight bytes.	0x0	R/W
1	MAC_IF_RX_SOP_SFD_EN	Enable RX SOP Signal Indication on SFD Reception. If both MAC_IF_RX_SOP_DET_EN and MAC_IF_RX_SOP_SFD_EN are set, the RX SOP signal is set when the SFD is received. Otherwise, the RX SOP is set when RX_DV is set. The RX SOP signal remains set until the end of the frame.	0x1	R/W
0	MAC_IF_RX_SOP_DET_EN	Enable the Generation of the RX SOP Indication Signal.	0x1	R/W

PCB LAYOUT RECOMMENDATIONS

LAND PATTERN

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical, electrical, and thermal reasons.

For thermal impedance performance and to maximize heat transfer to the PCB, the use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended. Via tenting is also recommended.

COMPONENT PLACEMENT AND ROUTING

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout. The critical components are the crystal and load capacitors, the CEXT_2 and CEXT_3 capacitors, and all bypass capacitors local to the ADIN1100 device. Prioritize these components for placement and routing.

- Place the decoupling capacitor as close as possible to their input pins.
- Minimize traces turns, and use a 45° corner.
- Avoid traces crossing power planes on adjacent layers.
- Avoid stubs.
- Keep the MDI traces (RXP, RXN, TXP, and TXN) as short as possible.
- Avoid vias on a high speed signal. Place ground vias next to the signal vias to improve the return current path.

CRYSTAL PLACEMENT AND ROUTING

Particular attention is required on the crystal placement and routing to ensure minimum current consumption, reduce stray capacitance, and improve noise immunity.

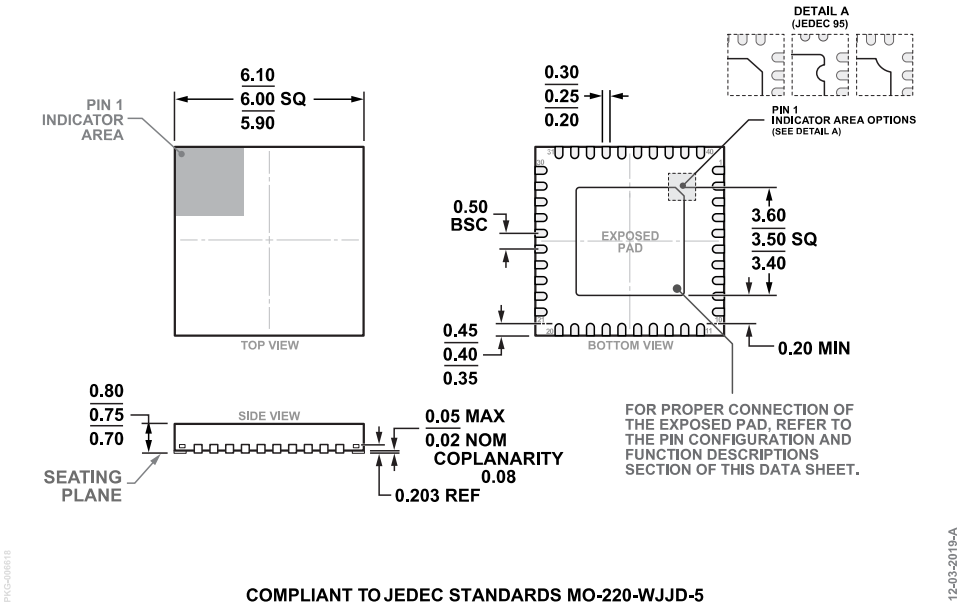
- Place the crystal, capacitors as close as possible to the ADIN1100 XTAL_I/CLK_IN and XTAL_O pins.
- Place the load capacitors close to each other.
- Use a local GND plane (copper island) for the crystal and load capacitors with a single point connection to the main GND.
- Reduce parasitic capacitance by keeping the XTAL_I and XTAL_O traces away from each other.
- Adding a copper keepout on the layer beneath the crystal can also reduce the parasitic capacitance.

PCB STACK

Follow these recommendations for the PCB stack:

- Use a PCB stack with a minimum of four layers. Consider six layers or more with external layers used as ground planes to improve EMI issues (optional).
- Define copper layer thickness based on the application and power requirements.
- Use internal layers for the power and ground planes.
- Use external layers for the signal traces.
- Use via stitching to improve ground and reduce EMI. The stitching pattern and via to via gaps are defined based on the application.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

Figure 31. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-29)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADIN1100BCPZ	-40°C to +85°C	40-Lead LFCSP	Tray, 490	CP-40-29
ADIN1100BCPZ-R7	-40°C to +85°C	40-Lead LFCSP	Reel, 750	CP-40-29
ADIN1100CCPZ	-40°C to +105°C	40-Lead LFCSP	Tray 490	CP-40-29
ADIN1100CCPZ-R7	-40°C to +105°C	40-Lead LFCSP	Reel, 750	CP-40-29

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Package Description
EVAL-ADIN1100EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.