

# MCF8316A 无传感器磁场定向控制 (FOC) 集成 FET BLDC 驱动器

## 1 特性

- 采用集成无传感器电机控制算法的三相 BLDC 电机驱动器
  - 无代码场定向控制 (FOC)
  - 使用电机参数提取工具 (MPET) 离线测量电机参数
  - 5 点可配置速度配置文件支持
  - 通过正向重新同步和反向驱动支持风力机
  - 模拟, PWM, 频率或基于 I<sup>2</sup>C 的速度输入
  - 可配置的电机启动和停止选项
  - 抗电压浪涌保护可防止过压
  - 通过自动死区时间补偿提高了声学性能
- 4.5V 至 35V 工作电压 (绝对最大值 40V)
- 高输出电流能力: 8A 峰值
- 低 MOSFET 导通状态电阻
  - T<sub>A</sub> = 25°C 时, R<sub>DS(ON)</sub> (HS + LS) 为 95mΩ
- 低功耗睡眠模式
  - V<sub>VM</sub> = 24V, T<sub>A</sub> = 25°C 时为 3μA (最大值)
- 速度环路精度: 3% 使用内部时钟, 1% 使用外部时钟参考
- 用于存储器件配置的客户可配置非易失性存储器 (EEPROM)
- 支持高达 75kHz 的 PWM 频率, 以支持低电感电机
- 不需要外部电流检测电阻器, 内置电流感测功能
- 内置 3.3V ±5%、20mA LDO 稳压器
- 内置 3.3V/5V、170mA 降压稳压器
- 专用 DRV0FF 引脚以禁用 (高阻态) 输出
- 展频和压摆率, 用于降低 EMI
- 整套集成保护特性
  - 电源欠压锁定 (UVLO)
  - 电机锁定检测 (5 种不同类型)
  - 过流保护 (OCP)
  - 热警告和热关断 (OTW/TSD)
  - 故障条件指示引脚 (nFAULT)
  - 可选择通过 I<sup>2</sup>C 接口进行故障诊断

能够为器件生成 3.3V 或 5.0V 电压轨, 可用于为外部电路供电。

算法配置可存储在非易失性 EEPROM 中, 从而允许器件在配置后独立运行。该器件通过 PWM 输入、模拟电压、可变频率方波或 I<sup>2</sup>C 命令接收速度命令。MCF8316A 集成多种保护特性, 旨在出现故障事件时保护该器件、电机和系统。

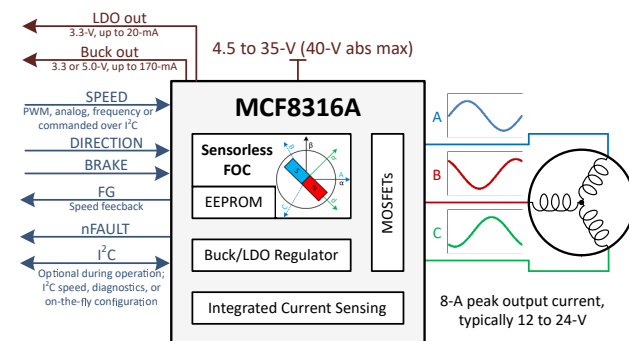
### 器件信息(1)

| 器件型号       | 封装        | 封装尺寸 (标称值)      |
|------------|-----------|-----------------|
| MCF8316A1V | VQFN (40) | 7.00mm x 5.00mm |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

### 参考文档:

- 请参阅 [E2E 常见问题解答](#) 中的阐释。
- 请参阅 [MCF8316A 调优指南](#)
- 请参阅 [MCF8316A EVM GUI](#)



简化版原理图

## 2 应用

- 无刷直流 (BLDC) 电机模块
- 住宅和起居风扇
- 空气净化器和加湿器风扇
- 洗衣机和洗碗机泵
- 汽车风扇和风机
- 医用 CPAP 风机

## 3 说明

MCF8316A 为驱动峰值电流高达 8A 的速度受控型 12V 至 24V 无刷直流电机 (BLDC) 或永磁同步电机 (PMSM) 的客户提供了一个单芯片无代码无传感器 FOC 解决方案。MCF8316A 集成了三个 1/2H 桥, 具有 40V 的绝对最大电压和 95mΩ 的超低 R<sub>DS(ON)</sub> (高侧 + 低侧)。可调降压稳压器和 LDO 的电源管理系列



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## 4 Revision History

| Changes from Revision A (December 2021) to Revision B (February 2022) | Page |
|---|------|
| • 更新了 E2E 链接.....   | 1    |

| Changes from Revision * (August 2021) to Revision A (December 2021) | Page |
|---|------|
| • 将器件状态更新为“量产数据”.....   | 1    |

## 5 Pin Configuration and Functions

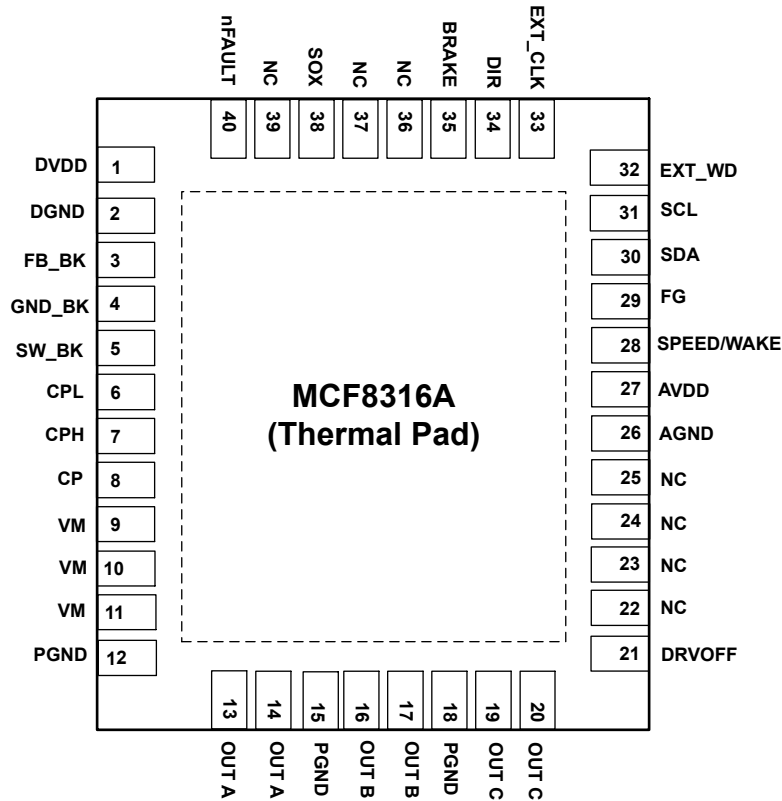


图 5-1. MCF8316A 40-Pin VQFN With Exposed Thermal Pad Top View

表 5-1. Pin Functions

| PIN     | 40-pin Package | TYPE <sup>(1)</sup> | DESCRIPTION  |
|---------|----------------|---------------------|--|
| NAME    | MCF8316A       |                     |  |
| AGND    | 26             | GND                 | Device analog ground. Refer <a href="#">Layout Guidelines</a> for connections recommendation.  |
| AVDD    | 27             | PWR O               | 3.3-V internal regulator output. Connect a X5R or X7R, 1- $\mu$ F, 6.3-V ceramic capacitor between the AVDD1 and AGND pins. This regulator can source up to 20 mA externally.  |
| BRAKE   | 35             | I                   | High $\rightarrow$ Brake the motor when High<br>Low $\rightarrow$ normal operation<br>Connect to PGND via 10-k $\Omega$ resistor, if not used  |
| CP      | 8              | PWR                 | Charge pump output. Connect a X5R or X7R, 1- $\mu$ F, 16-V ceramic capacitor between the CP and VM pins.   |
| CPH     | 7              | PWR                 | Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.   |
| CPL     | 6              | PWR                 |  |
| DGND    | 2              | GND                 | Device digital ground. Refer <a href="#">Layout Guidelines</a> for connections recommendation.   |
| DIR     | 34             | I                   | Direction of motor spinning;<br>When low, phase driving sequence is OUT A $\rightarrow$ OUT C $\rightarrow$ OUT B<br>When high, phase driving sequence is OUT A $\rightarrow$ OUT B $\rightarrow$ OUT C<br>Connect to AVDD via 10-k $\Omega$ resistor, if not used |
| DRVOFF  | 21             | I                   | Coast (Hi-Z) all six MOSFETs when DRVOFF is high.  |
| DVDD    | 1              | PWR                 | 1.5-V internal regulator output. Connect a X5R or X7R, 1- $\mu$ F, 6.3-V ceramic capacitor between the DVDD and DGND pins.   |
| EXT_CLK | 33             | I                   | External clock reference input in external clock reference mode.   |
| EXT_WD  | 32             | I                   | External watchdog input.   |

表 5-1. Pin Functions (continued)

| PIN<br>NAME    | 40-pin Package<br>MCF8316A    | TYPE <sup>(1)</sup> | DESCRIPTION  |
|----------------|-------------------------------|---------------------|--|
| FB_BK          | 3                             | PWR I/O             | Feedback for buck regulator output control. Connect to buck regulator output after the inductor/resistor.  |
| FG             | 29                            | O                   | Motor speed indicator output. Open-drain output requires an external pull-up resistor to 1.8 to 5-V.   |
| GND_BK         | 4                             | GND                 | Buck regulator ground. Refer <a href="#">Layout Guidelines</a> for connections recommendation.   |
| NC             | 22, 23, 24, 25, 36,<br>37, 39 | -                   | No connection, open  |
| nFAULT         | 40                            | O                   | Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V.   |
| OUTA           | 13, 14                        | PWR O               | Half bridge output A   |
| OUTB           | 16, 17                        | PWR O               | Half bridge output B   |
| OUTC           | 19, 20                        | PWR O               | Half bridge output C   |
| PGND           | 12, 15, 18                    | GND                 | Device power ground. Refer <a href="#">Layout Guidelines</a> for connections recommendation.   |
| SCL            | 31                            | I                   | I <sup>2</sup> C clock input   |
| SDA            | 30                            | I/O                 | I <sup>2</sup> C data line   |
| SPEED/<br>WAKE | 28                            | I                   | Device speed input; supports analog, PWM or frequency based speed input. The speed pin input can be configured through SPEED_MODE.   |
| SOX            | 38                            | O                   | CSA output from one of the three phases depending on configuration - SOA, SOB or SOC.  |
| SW_BK          | 5                             | PWR                 | Buck switch node. Connect this pin to an inductor or resistor.   |
| VM             | 9, 10, 11                     | PWR I               | Device and motor power supply. Connect to motor supply voltage; bypass to GND with one 0.1- $\mu$ F capacitor plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device. |
| Thermal pad    |                               | GND                 | Must be connected to ground.   |

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|  | MIN  | MAX                   | UNIT |
|--|------|-----------------------|------|
| Power supply pin voltage (VM)  | -0.3 | 40                    | V    |
| Power supply voltage ramp (VM)   |      | 4                     | V/μs |
| Voltage difference between ground pins (GND_BK, DGND, PGND, AGND)              | -0.3 | 0.3                   | V    |
| Charge pump voltage (CPH, CP)  | -0.3 | V <sub>VM</sub> + 6   | V    |
| Charge pump negative switching pin voltage (CPL)                               | -0.3 | V <sub>VM</sub> + 0.3 | V    |
| Switching regulator pin voltage (FB_BK)  | -0.3 | 5.75                  | V    |
| Switching node pin voltage (SW_BK)   | -0.3 | V <sub>VM</sub> + 0.3 | V    |
| Analog regulators pin voltage (AVDD)   | -0.3 | 4                     | V    |
| Analog regulators pin voltage (DVDD)   | -0.3 | 1.7                   | V    |
| Logic pin input voltage (BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED) | -0.3 | 6                     | V    |
| Open drain pin output voltage (nFAULT, FG)                                     | -0.3 | 6                     | V    |
| Output pin voltage (OUTA, OUTB, OUTC)  | -1   | V <sub>VM</sub> + 1   | V    |
| Ambient temperature, T <sub>A</sub>  | -40  | 125                   | °C   |
| Junction temperature, T <sub>J</sub>   | -40  | 150                   | °C   |
| Storage temperature, T <sub>stg</sub>  | -65  | 150                   | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

### 6.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>         | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JS-002 <sup>(2)</sup> | ±750  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                                 |                                      |  | MIN  | NOM | MAX | UNIT |
|---------------------------------|--------------------------------------|--|------|-----|-----|------|
| V <sub>VM</sub>                 | Power supply voltage                 | V <sub>VM</sub>                                      | 4.5  | 24  | 35  | V    |
| I <sub>OUT</sub> <sup>(1)</sup> | Peak output winding current          | OUTA, OUTB, OUTC                                     |      |     | 8   | A    |
| V <sub>IN_LOGIC</sub>           | Logic input voltage                  | BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SPEED, SDA, SCL | -0.1 |     | 5.5 | V    |
| V <sub>OD</sub>                 | Open drain pullup voltage            | nFAULT, FG   | -0.1 |     | 5.5 | V    |
| I <sub>OD</sub>                 | Open drain output current capability | nFAULT, FG   |      |     | 5   | mA   |
| T <sub>A</sub>                  | Operating ambient temperature        |  | -40  |     | 125 | °C   |
| T <sub>J</sub>                  | Operating Junction temperature       |  | -40  |     | 150 | °C   |

- (1) Power dissipation and thermal limits must be observed

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | MCF8316A   | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RGF (VQFN) |      |
|                               |  | 40 Pins    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 25.7       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 15.2       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 7.3        | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 7.2        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 2.0        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at T<sub>J</sub> = –40°C to +150°C, V<sub>VM</sub> = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>VM</sub> = 24 V

| PARAMETER             |                                 | TEST CONDITIONS  | MIN   | TYP  | MAX   | UNIT |
|-----------------------|---------------------------------|--|-------|------|-------|------|
| <b>POWER SUPPLIES</b> |                                 |  |       |      |       |      |
| I <sub>VMQ</sub>      | VM sleep mode current           | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> = 0, T <sub>A</sub> = 25 °C  |       | 3    | 5     | μA   |
|                       |                                 | V <sub>SPEED</sub> = 0, T <sub>A</sub> = 125 °C  |       | 3.5  | 7     | μA   |
| I <sub>VMS</sub>      | VM standby mode current         | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, T <sub>A</sub> = 25 °C, L <sub>BK</sub> = 47 uH, C <sub>BK</sub> = 22 μF                                     |       | 8    | 15    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF  |       | 25   | 28    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, L <sub>BK</sub> = 47 uH, C <sub>BK</sub> = 22 μF   |       | 8    | 15    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF  |       | 25   | 28    | mA   |
| I <sub>VM</sub>       | VM operating mode current       | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), T <sub>J</sub> = 25 °C, L <sub>BK</sub> = 47 uH, C <sub>BK</sub> = 22 μF, No Motor Connected |       | 11   | 18    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), T <sub>J</sub> = 25 °C, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF, No Motor Connected  |       | 27   | 30    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), L <sub>BK</sub> = 47 uH, C <sub>BK</sub> = 22 μF, No Motor Connected                         |       | 11   | 17    | mA   |
|                       |                                 | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF, No Motor Connected                          |       | 28   | 30    | mA   |
| V <sub>AVDD</sub>     | Analog regulator voltage        | 0 mA ≤ I <sub>AVDD</sub> ≤ 30 mA   | 3.125 | 3.3  | 3.465 | V    |
| I <sub>AVDD</sub>     | External analog regulator load  |  |       |      | 20    | mA   |
| V <sub>DVDD</sub>     | Digital regulator voltage       |  | 1.4   | 1.55 | 1.65  | V    |
| V <sub>VCP</sub>      | Charge pump regulator voltage   | VCP with respect to VM   | 4.0   | 4.7  | 5.5   | V    |
| f <sub>CP</sub>       | Charge pump switching frequency |  |       | 400  |       | kHz  |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$ 

| PARAMETER             |   | TEST CONDITIONS  | MIN  | TYP                                       | MAX                 | UNIT |
|-----------------------|---|--|------|---|---------------------|------|
| <b>BUCK REGULATOR</b> |   |  |      |   |                     |      |
| $V_{BK}$              | Buck regulator average voltage<br>( $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ) | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 00b   | 3.1  | 3.3                                       | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 01b   | 4.6  | 5.0                                       | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 10b   | 3.7  | 4.0                                       | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 11b   | 5.2  | 5.7                                       | 6.2                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b) or $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 11b),<br>$0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$                   |      | $V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ (1) |                     | V    |
| $V_{BK}$              | Buck regulator average voltage<br>( $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ) | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 00b  | 3.1  | 3.3                                       | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 01b  | 4.6  | 5.0                                       | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 10b  | 3.7  | 4.0                                       | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 11b  | 5.2  | 5.7                                       | 6.2                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b) or $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 11b),<br>$0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$                    |      | $V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ (1) |                     | V    |
| $V_{BK}$              | Buck regulator average voltage<br>( $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ )      | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 00b  | 3.1  | 3.3                                       | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 01b  | 4.6  | 5.0                                       | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 10b  | 3.7  | 4.0                                       | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 11b  | 5.2  | 5.7                                       | 6.2                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b) or $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 11b),<br>$0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$                    |      | $V_{VM} - I_{BK} \cdot (R_{BK} + 2)$      |                     | V    |
| $V_{BK\_RIP}$         | Buck regulator ripple voltage   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ , Buck<br>regulator with inductor, $L_{BK} = 47\ \mu\text{H}$ , $C_{BK}$<br>$= 22\ \mu\text{F}$ | -100 |   | 100                 | mV   |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ , Buck<br>regulator with inductor, $L_{BK} = 22\ \mu\text{H}$ , $C_{BK}$<br>$= 22\ \mu\text{F}$  | -100 |   | 100                 | mV   |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ , Buck<br>regulator with resistor; $R_{BK} = 22\ \Omega$ , $C_{BK}$<br>$= 22\ \mu\text{F}$       | -100 |   | 100                 | mV   |
| $I_{BK}$              | External buck regulator load  | $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b  |      |   | 170                 | mA   |
|                       |   | $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b  |      |   | 170 –<br>$I_{AVDD}$ | mA   |
|                       |   | $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b  |      |   | 20                  | mA   |
|                       |   | $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b  |      |   | 20 –<br>$I_{AVDD}$  | mA   |
|                       |   | $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b   |      |   | 10                  | mA   |
|                       |   | $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b   |      |   | 10 –<br>$I_{AVDD}$  | mA   |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                |   | TEST CONDITIONS  | MIN | TYP  | MAX  | UNIT       |
|--------------------------|---|--|-----|------|------|------------|
| $f_{\text{SW\_BK}}$      | Buck regulator switching frequency                                    | Regulation Mode  | 20  |      | 535  | kHz        |
|                          |   | Linear Mode  | 20  |      | 535  | kHz        |
| $V_{\text{BK\_UV}}$      | Buck regulator undervoltage lockout                                   | $V_{\text{BK}}$ rising, BUCK_SEL = 00b   | 2.7 | 2.8  | 2.95 | V          |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 00b  | 2.5 | 2.6  | 2.7  | V          |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 01b   | 4.3 | 4.4  | 4.55 | V          |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 01b  | 4.1 | 4.2  | 4.35 | V          |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 10b   | 2.7 | 2.8  | 2.95 | V          |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 10b  | 2.5 | 2.6  | 2.7  | V          |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 11b   | 4.3 | 4.4  | 4.55 | V          |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 11b  | 4.1 | 4.2  | 4.35 | V          |
| $V_{\text{BK\_UV\_HYS}}$ | Buck regulator undervoltage lockout hysteresis                        | Rising to falling threshold  | 90  | 200  | 400  | mV         |
| $I_{\text{BK\_CL}}$      | Buck regulator Current limit threshold                                | BUCK_CL = 0b   | 360 | 600  | 910  | mA         |
|                          |   | BUCK_CL = 1b   | 80  | 150  | 250  | mA         |
| $I_{\text{BK\_OCP}}$     | Buck regulator Overcurrent protection trip point                      |  | 2   | 3    | 4    | A          |
| $t_{\text{BK\_RETRY}}$   | Overcurrent protection retry time                                     |  | 0.7 | 1    | 1.3  | ms         |
| <b>DRIVER OUTPUTS</b>    |   |  |     |      |      |            |
| $R_{\text{DS(ON)}}$      | Total MOSFET on resistance (High-side + Low-side)                     | $V_{\text{VM}} > 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_A = 25^\circ\text{C}$  |     | 95   | 125  | m $\Omega$ |
|                          |   | $V_{\text{VM}} < 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_A = 25^\circ\text{C}$  |     | 105  | 130  | m $\Omega$ |
|                          |   | $V_{\text{VM}} > 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_J = 150^\circ\text{C}$ |     | 140  | 185  | m $\Omega$ |
|                          |   | $V_{\text{VM}} < 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_J = 150^\circ\text{C}$ |     | 145  | 190  | m $\Omega$ |
| SR                       | Phase pin slew rate switching low to high (Rising from 20 % to 80 %)  | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 00b  | 13  | 25   | 45   | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 01b  | 30  | 50   | 80   | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 10b  | 80  | 125  | 185  | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 11b  | 130 | 200  | 280  | V/us       |
| SR                       | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 00b  | 14  | 25   | 45   | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 01b  | 30  | 50   | 80   | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 10b  | 80  | 125  | 185  | V/us       |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 11b  | 110 | 200  | 280  | V/us       |
| $t_{\text{DEAD}}$        | Output dead time (high to low / low to high)                          | $V_{\text{VM}} = 24\text{ V}$ , SR = 25 V/ $\mu\text{s}$                                 |     | 1800 | 3400 | ns         |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SR = 50 V/ $\mu\text{s}$                                 |     | 1100 | 1550 | ns         |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SR = 125 V/ $\mu\text{s}$                                |     | 650  | 1000 | ns         |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SR = 200 V/ $\mu\text{s}$                                |     | 500  | 750  | ns         |



at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                           |   | TEST CONDITIONS  | MIN   | TYP  | MAX   | UNIT          |
|-------------------------------------|---|--|-------|------|-------|---------------|
| <b>SPEED INPUT - PWM MODE</b>       |   |  |       |      |       |               |
| $f_{\text{PWM}}$                    | PWM input frequency   |  | 0.01  |      | 95    | kHz           |
| $\text{Res}_{\text{PWM}}$           | PWM input resolution  | $f_{\text{PWM}} = 0.01$ to $0.35\text{ kHz}$   | 11    | 12   | 13    | bits          |
|                                     |   | $f_{\text{PWM}} = 0.35$ to $2\text{ kHz}$  | 12    | 13   | 14    | bits          |
|                                     |   | $f_{\text{PWM}} = 2$ to $3.5\text{ kHz}$   | 11    | 11.5 | 12    | bits          |
|                                     |   | $f_{\text{PWM}} = 3.5$ to $7\text{ kHz}$   | 13    | 13.5 | 14    | bits          |
|                                     |   | $f_{\text{PWM}} = 7$ to $14\text{ kHz}$  | 12    | 12.5 | 13    | bits          |
|                                     |   | $f_{\text{PWM}} = 14$ to $29.2\text{ kHz}$   | 11    | 11.5 | 12    | bits          |
|                                     |   | $f_{\text{PWM}} = 29.3$ to $60\text{ kHz}$   | 10    | 10.5 | 11    | bits          |
|                                     |   | $f_{\text{PWM}} = 60$ to $95\text{ kHz}$   | 8     | 9    | 10    | bits          |
| <b>SPEED INPUT - ANALOG MODE</b>    |   |  |       |      |       |               |
| $V_{\text{ANA\_FS}}$                | Analog full-speed voltage                                       |  | 2.95  | 3    | 3.05  | V             |
| $V_{\text{ANA\_RES}}$               | Analog voltage resolution                                       |  |       | 732  |       | $\mu\text{V}$ |
| <b>SPEED INPUT - FREQUENCY MODE</b> |   |  |       |      |       |               |
| $f_{\text{PWM\_FREQ}}$              | PWM input frequency range                                       | Duty cycle = 50%   | 3     |      | 32767 | Hz            |
| <b>SLEEP MODE</b>                   |   |  |       |      |       |               |
| $V_{\text{EN\_SL}}$                 | Analog voltage to enter sleep mode                              | $\text{SPEED\_MODE} = 00\text{b}$ (analog mode)  |       |      | 40    | mV            |
| $V_{\text{EX\_SL}}$                 | Analog voltage to exit sleep mode                               | $\text{SPEED\_MODE} = 00\text{b}$ (analog mode)  | 2.2   |      |       | V             |
| $t_{\text{DET\_ANA}}$               | Time needed to detect wake up signal on SPEED pin               | $\text{SPEED\_MODE} = 00\text{b}$ (analog mode)<br>$V_{\text{SPEED}} > V_{\text{EX\_SL}}$  | 0.5   | 1    | 1.5   | $\mu\text{s}$ |
| $t_{\text{WAKE}}$                   | Wakeup time from sleep mode                                     | $V_{\text{SPEED}} > V_{\text{EX\_SL}}$ to DVDD voltage available, $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)                     |       | 3    | 5     | ms            |
| $t_{\text{EX\_SL\_DR\_ANA}}$        | Time taken to drive motor after exiting from sleep mode         | $\text{SPEED\_MODE} = 00\text{b}$ (analog mode)<br>$V_{\text{SPEED}} > V_{\text{EN\_SL}}$ , ISD detection disabled                 |       |      | 20    | ms            |
| $t_{\text{DET\_PWM}}$               | Time needed to detect wake up signal on SPEED pin               | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} > V_{\text{DIG\_IH}}$  | 0.5   | 1    | 1.5   | $\mu\text{s}$ |
| $t_{\text{WAKE\_PWM}}$              | Wakeup time from sleep mode                                     | $V_{\text{SPEED}} > V_{\text{DIG\_IH}}$ to DVDD voltage available and release nFault, $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode) |       | 3    | 5     | ms            |
| $t_{\text{EX\_SL\_DR\_PWM}}$        | Time taken to drive motor after wakeup from sleep state         | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} > V_{\text{DIG\_IH}}$ , ISD detection disabled                   |       |      | 20    | ms            |
| $t_{\text{DET\_SL\_ANA}}$           | Time needed to detect sleep command                             | $\text{SPEED\_MODE} = 00\text{b}$ (analog mode)<br>$V_{\text{SPEED}} < V_{\text{EN\_SL}}$  | 0.5   | 1    | 2     | ms            |
| $t_{\text{DET\_SL\_PWM}}$           | Time needed to detect sleep command                             | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} < V_{\text{DIG\_IL}}$ , $\text{SLEEP\_ENTRY\_TIME} = 00\text{b}$ | 0.035 | 0.05 | 0.065 | ms            |
|                                     |   | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} < V_{\text{DIG\_IL}}$ , $\text{SLEEP\_ENTRY\_TIME} = 01\text{b}$ | 0.14  | 0.2  | 0.26  | ms            |
|                                     |   | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} < V_{\text{DIG\_IL}}$ , $\text{SLEEP\_ENTRY\_TIME} = 10\text{b}$ | 14    | 20   | 26    | ms            |
|                                     |   | $\text{SPEED\_MODE} = 01\text{b}$ (PWM mode)<br>$V_{\text{SPEED}} < V_{\text{DIG\_IL}}$ , $\text{SLEEP\_ENTRY\_TIME} = 11\text{b}$ | 140   | 200  | 260   | ms            |
| $t_{\text{DET\_SL\_FREQ}}$          | Time needed to detect sleep command                             | $\text{SPEED\_MODE} = 11\text{b}$ (Frequency mode)<br>$V_{\text{SPEED}} < V_{\text{DIG\_IL}}$                                      |       | 4000 |       | ms            |
| $t_{\text{EN\_SL}}$                 | Time needed to stop driving motor after detecting sleep command | $V_{\text{SPEED}} < V_{\text{EN\_SL}}$ (analog mode) or $V_{\text{SPEED}} < V_{\text{DIG\_IL}}$ (PWM mode)                         |       | 1    | 2     | ms            |

at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 24\text{ V}$ 

| PARAMETER  |   | TEST CONDITIONS  | MIN                  | TYP                 | MAX                  | UNIT          |
|--|---|--|----------------------|---------------------|----------------------|---------------|
| <b>STANDBY MODE</b>  |   |  |                      |                     |                      |               |
| $V_{EN\_SB}$   | Analog voltage to enter standby mode                              | SPEED_MODE = 00b (analog mode)   |                      |                     | 40                   | mV            |
| $V_{EX\_SB}$   | Analog voltage to exit standby mode                               | SPEED_MODE = 00b (analog mode)   | 170                  |                     |                      | mV            |
| $t_{EX\_SB\_DR\_A\_NA}$  | Time taken to drive motor after exiting standby mode              | SPEED_MODE = 00b (analog mode)<br>$V_{SPEED} > V_{EN\_SB}$ , ISD detection disabled                        |                      |                     | 6                    | ms            |
| $t_{EX\_SB\_DR\_P\_WM}$  | Time taken to drive motor after exiting standby mode              | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} > V_{DIG\_IH}$ , ISD detection disabled                          |                      |                     | 6                    | ms            |
| $t_{DET\_SB\_ANA}$   | Time needed to detect standby mode                                | SPEED_MODE = 00b (analog mode)<br>$V_{SPEED} < V_{EN\_SB}$   | 0.5                  | 1                   | 2                    | ms            |
| $t_{EN\_SB\_PWM}$  | Time needed to detect standby command                             | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{DIG\_IL}$ , SLEEP_ENTRY_TIME = 00b                          | 0.035                | 0.05                | 0.065                | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{DIG\_IL}$ , SLEEP_ENTRY_TIME = 01b                          | 0.14                 | 0.2                 | 0.26                 | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{DIG\_IL}$ , SLEEP_ENTRY_TIME = 10b                          | 14                   | 20                  | 26                   | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{DIG\_IL}$ , SLEEP_ENTRY_TIME = 11b                          | 140                  | 200                 | 260                  | ms            |
| $t_{EN\_SB\_FREQ}$   | Time needed to detect standby mode                                | SPEED_MODE = 11b (Frequency mode), $V_{SPEED} < V_{DIG\_IL}$   |                      | 4000                |                      | ms            |
| $t_{EN\_SB\_DIG}$  | Time needed to detect standby mode                                | SPEED_MODE = 10b (I2C mode), SPEED_CMD = 0   |                      | 1                   | 2                    | ms            |
| $t_{EN\_SB}$   | Time needed to stop driving motor after detecting standby command | $V_{SPEED} < V_{EN\_SL}$ (analog mode) or $V_{SPEED} < V_{DIG\_IL}$ (PWM mode) or SPEED_CMD = 0 (I2C mode) |                      | 1                   | 2                    | ms            |
| <b>LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)</b> |   |  |                      |                     |                      |               |
| $V_{IL}$   | Input logic low voltage   | AVDD = 3 to 3.6 V  |                      |                     | $0.25 \cdot AV_{DD}$ | V             |
| $V_{IH}$   | Input logic high voltage  | AVDD = 3 to 3.6 V  | $0.65 \cdot AV_{DD}$ |                     |                      | V             |
| $V_{HYS}$  | Input hysteresis  |  | 50                   | 500                 | 800                  | mV            |
| $I_{IL}$   | Input logic low current   | AVDD = 3 to 3.6 V  | -0.15                |                     | 0.15                 | $\mu\text{A}$ |
| $I_{IH}$   | Input logic high current  | AVDD = 3 to 3.6 V  | -0.3                 |                     | 0                    | $\mu\text{A}$ |
| $R_{PD\_SPEED}$  | Input pulldown resistance   | SPEED pin To GND   | 0.6                  | 1                   | 1.4                  | M $\Omega$    |
| $R_{PD}$   | Input pulldown resistance   | To GND   | 90                   | 100                 | 110                  | k $\Omega$    |
| <b>OPEN-DRAIN OUTPUTS (nFAULT, FG)</b>                                   |   |  |                      |                     |                      |               |
| $V_{OL}$   | Output logic low voltage  | $I_{OD} = -5\text{ mA}$  |                      |                     | 0.4                  | V             |
| $I_{OZ}$   | Output logic high current   | $V_{OD} = 3.3\text{ V}$  | 0                    |                     | 0.5                  | $\mu\text{A}$ |
| <b>I<sup>2</sup>C Serial Interface</b>                                   |   |  |                      |                     |                      |               |
| $V_{I2C\_L}$   | LOW-level input voltage   |  | -0.5                 | $0.3 \cdot AV_{DD}$ |                      | V             |
| $V_{I2C\_H}$   | HIGH-level input voltage  |  | $0.7 \cdot AV_{DD}$  |                     | 5.5                  | V             |
| $V_{I2C\_HYS}$   | Hysteresis  |  | $0.05 \cdot AV_{DD}$ |                     |                      | V             |
| $V_{I2C\_OL}$  | LOW-level output voltage  | open-drain at 2mA sink current   | 0                    |                     | 0.4                  | V             |
| $I_{I2C\_OL}$  | LOW-level output current  | $V_{I2C\_OL} = 0.6\text{ V}$   |                      |                     | 6                    | mA            |
| $I_{I2C\_IL}$  | Input current on SDA and SCL                                      |  | -10 <sup>(2)</sup>   |                     | 10 <sup>(2)</sup>    | $\mu\text{A}$ |
| $C_i$  | Capacitance for SDA and SCL                                       |  |                      |                     | 10                   | pF            |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                  |  | TEST CONDITIONS                          | MIN  | TYP   | MAX                | UNIT          |
|----------------------------|--|--|------|-------|--------------------|---------------|
| $t_{of}$                   | Output fall time from $V_{I2C\_H}(\text{min})$ to $V_{I2C\_L}(\text{max})$ | Standard Mode                            |      |       | 250 <sup>(3)</sup> | ns            |
|                            |  | Fast Mode                                |      |       | 250 <sup>(3)</sup> | ns            |
| $t_{SP}$                   | Pulse width of spikes that must be suppressed by the input filter          | Fast Mode                                | 0    |       | 50 <sup>(4)</sup>  | ns            |
| <b>OSCILLATOR</b>          |  |  |      |       |                    |               |
| $f_{OSCREF}$               | External clock reference   | EXT_CLK_CONFIG = 000b                    |      | 8     |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 001b                    |      | 16    |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 010b                    |      | 32    |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 011b                    |      | 64    |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 100b                    |      | 128   |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 101b                    |      | 256   |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 110b                    |      | 512   |                    | kHz           |
|                            |  | EXT_CLK_CONFIG = 111b                    |      | 1024  |                    | kHz           |
| <b>EEPROM</b>              |  |  |      |       |                    |               |
| $EE_{Prog}$                | Programing voltage   |  | 1.35 | 1.5   | 1.65               | V             |
| $EE_{RET}$                 | Retention  | $T_A = 25^\circ\text{C}$                 |      | 100   |                    | Years         |
|                            |  | $T_J = -40$ to $150^\circ\text{C}$       |      | 10    |                    | Years         |
| $EE_{END}$                 | Endurance  | $T_J = -40$ to $150^\circ\text{C}$       |      | 1000  |                    | Cycles        |
|                            |  | $T_J = -40$ to $85^\circ\text{C}$        |      | 20000 |                    | Cycles        |
| <b>PROTECTION CIRCUITS</b> |  |  |      |       |                    |               |
| $V_{UVLO}$                 | Supply undervoltage lockout (UVLO)   | VM rising                                | 4.3  | 4.4   | 4.5                | V             |
|                            |  | VM falling                               | 4.1  | 4.2   | 4.3                | V             |
| $V_{UVLO\_HYS}$            | Supply undervoltage lockout hysteresis                                     | Rising to falling threshold              | 140  | 200   | 350                | mV            |
| $t_{UVLO}$                 | Supply undervoltage deglitch time  |  | 3    | 5     | 7                  | $\mu\text{s}$ |
| $V_{OVP}$                  | Supply overvoltage protection (OVP)  | Supply rising, OVP_EN = 1, OVP_SEL = 0   | 32.5 | 34    | 35                 | V             |
|                            |  | Supply falling, OVP_EN = 1, OVP_SEL = 0  | 31.8 | 33    | 34.3               | V             |
|                            |  | Supply rising, OVP_EN = 1, OVP_SEL = 1   | 20   | 22    | 23                 | V             |
|                            |  | Supply falling, OVP_EN = 1, OVP_SEL = 1  | 19   | 21    | 22                 | V             |
| $V_{OVP\_HYS}$             | Supply overvoltage protection (OVP)  | Rising to falling threshold, OVP_SEL = 1 | 0.9  | 1     | 1.1                | V             |
|                            |  | Rising to falling threshold, OVP_SEL = 0 | 0.7  | 0.8   | 0.9                | V             |
| $t_{OVP}$                  | Supply overvoltage deglitch time   |  | 2.5  | 5     | 7                  | $\mu\text{s}$ |
| $V_{CPUV}$                 | Charge pump undervoltage lockout (above VM)                                | Supply rising                            | 2.25 | 2.5   | 2.75               | V             |
|                            |  | Supply falling                           | 2.2  | 2.4   | 2.6                | V             |
| $V_{CPUV\_HYS}$            | Charge pump UVLO hysteresis  | Rising to falling threshold              | 65   | 100   | 150                | mV            |
| $V_{AVDD\_UV}$             | Analog regulator undervoltage lockout                                      | Supply rising                            | 2.7  | 2.85  | 3                  | V             |
|                            |  | Supply falling                           | 2.5  | 2.65  | 2.8                | V             |
| $V_{AVDD\_UV\_HYS}$        | Analog regulator undervoltage lockout hysteresis                           | Rising to falling threshold              | 180  | 200   | 240                | mV            |
| $I_{OCP}$                  | Overcurrent protection trip point  | OCP_LVL = 0b                             | 10   | 16    | 20                 | A             |
|                            |  | OCP_LVL = 1b                             | 15   | 24    | 28                 | A             |

at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 24\text{ V}$ 

| PARAMETER             |                                      | TEST CONDITIONS           | MIN | TYP  | MAX | UNIT               |
|-----------------------|--------------------------------------|---------------------------|-----|------|-----|--------------------|
| $t_{\text{OCP}}$      | Overcurrent protection deglitch time | OCP_DEG = 00b             | 0.1 | 0.3  | 0.7 | $\mu\text{s}$      |
|                       |                                      | OCP_DEG = 01b             | 0.2 | 0.6  | 1.2 | $\mu\text{s}$      |
|                       |                                      | OCP_DEG = 10b             | 0.6 | 1.25 | 1.8 | $\mu\text{s}$      |
|                       |                                      | OCP_DEG = 11b             | 1   | 1.6  | 2.5 | $\mu\text{s}$      |
| $t_{\text{RETRY}}$    | Overcurrent protection retry time    | OCP_RETRY = 0             | 4   | 5    | 6   | ms                 |
|                       |                                      | OCP_RETRY = 1             | 425 | 500  | 575 | ms                 |
| $T_{\text{OTW}}$      | Thermal warning temperature          | Die temperature ( $T_J$ ) | 160 | 170  | 180 | $^{\circ}\text{C}$ |
| $T_{\text{OTW\_HYS}}$ | Thermal warning hysteresis           | Die temperature ( $T_J$ ) | 25  | 30   | 35  | $^{\circ}\text{C}$ |
| $T_{\text{TSD}}$      | Thermal shutdown temperature         | Die temperature ( $T_J$ ) | 175 | 185  | 195 | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_HYS}}$ | Thermal shutdown hysteresis          | Die temperature ( $T_J$ ) | 25  | 30   | 35  | $^{\circ}\text{C}$ |
| $T_{\text{TSD}}$      | Thermal shutdown temperature (FET)   | Die temperature ( $T_J$ ) | 170 | 180  | 190 | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_HYS}}$ | Thermal shutdown hysteresis (FET)    | Die temperature ( $T_J$ ) | 20  | 25   | 30  | $^{\circ}\text{C}$ |

- (1)  $R_{\text{LBK}}$  is resistance of inductor  $L_{\text{BK}}$
- (2) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
- (3) The maximum  $t_f$  for the SDA and SCL bus lines (300 ns) is longer than the specified maximum  $t_{\text{of}}$  for the output stages (250 ns). This allows series protection resistors ( $R_s$ ) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- (4) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

## 6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

| PARAMETER            |  | TEST CONDITIONS                                       | MIN              | NOM | MAX                 | UNIT          |
|----------------------|--|---|------------------|-----|---------------------|---------------|
| <b>Standard-mode</b> |  |   |                  |     |                     |               |
| $f_{\text{SCL}}$     | SCL clock frequency  |   | 0                |     | 100                 | kHz           |
| $t_{\text{HD\_STA}}$ | Hold time (repeated) START condition   | After this period, the first clock pulse is generated | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{LOW}}$     | LOW period of the SCL clock  |   | 4.7              |     |                     | $\mu\text{s}$ |
| $t_{\text{HIGH}}$    | HIGH period of the SCL clock   |   | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{SU\_STA}}$ | Set-up time for a repeated START condition   |   | 4.7              |     |                     | $\mu\text{s}$ |
| $t_{\text{HD\_DAT}}$ | Data hold time <sup>(2)</sup>  | I2C bus devices                                       | 0 <sup>(3)</sup> |     | <sup>(4)</sup>      | $\mu\text{s}$ |
| $t_{\text{SU\_DAT}}$ | Data set-up time   |   | 250              |     |                     | ns            |
| $t_r$                | Rise time for both SDA and SCL signals   |   |                  |     | 1000                | ns            |
| $t_f$                | Fall time of both SDA and SCL signals <sup>(3)</sup><br><sup>(6)</sup> <sup>(7)</sup> <sup>(8)</sup> |   |                  |     | 300                 | ns            |
| $t_{\text{SU\_STO}}$ | Set-up time for STOP condition   |   | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{BUF}}$     | Bus free time between STOP and START condition   |   | 4.7              |     |                     | $\mu\text{s}$ |
| $C_b$                | Capacitive load for each bus line <sup>(9)</sup>   |   |                  |     | 400                 | pF            |
| $t_{\text{VD\_DAT}}$ | Data valid time <sup>(10)</sup>  |   |                  |     | 3.45 <sup>(4)</sup> | $\mu\text{s}$ |
| $t_{\text{VD\_ACK}}$ | Data valid acknowledge time <sup>(11)</sup>  |   |                  |     | 3.45 <sup>(4)</sup> | $\mu\text{s}$ |
| $V_{\text{nL}}$      | Noise margin at the LOW level  | For each connected device (including hysteresis)      | 0.1*AVD<br>D     |     |                     | V             |
| $V_{\text{nh}}$      | Noise margin at the HIGH level   | For each connected device (including hysteresis)      | 0.2*AVD<br>D     |     |                     | V             |
| <b>Fast-mode</b>     |  |   |                  |     |                     |               |
| $f_{\text{SCL}}$     | SCL clock frequency  |   | 0                |     | 400                 | KHz           |
| $t_{\text{HD\_STA}}$ | Hold time (repeated) START condition   | After this period, the first clock pulse is generated | 0.6              |     |                     | $\mu\text{s}$ |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           |  | TEST CONDITIONS                                  | MIN                     | NOM | MAX                | UNIT |
|---------------------|--|--|-------------------------|-----|--------------------|------|
| t <sub>LOW</sub>    | LOW period of the SCL clock  |  | 1.3                     |     |                    | μs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock   |  | 0.6                     |     |                    | μs   |
| t <sub>SU_STA</sub> | Set-up time for a repeated START condition                                     |  | 0.6                     |     |                    | μs   |
| t <sub>HD_DAT</sub> | Data hold time <sup>(2)</sup>  |  | 0 <sup>(3)</sup>        |     | <sup>(4)</sup>     | μs   |
| t <sub>SU_DAT</sub> | Data set-up time   |  | 100 <sup>(5)</sup>      |     |                    | ns   |
| t <sub>r</sub>      | Rise time for both SDA and SCL signals   |  | 20                      |     | 300                | ns   |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals <sup>(3)</sup><br><sup>(6) (7) (8)</sup> |  | 20 x<br>(AVDD/<br>5.5V) |     | 300                | ns   |
| t <sub>SU_STO</sub> | Set-up time for STOP condition   |  | 0.6                     |     |                    | μs   |
| t <sub>BUF</sub>    | Bus free time between STOP and START condition                                 |  | 1.3                     |     |                    | μs   |
| C <sub>b</sub>      | Capacitive load for each bus line <sup>(9)</sup>                               |  |                         |     | 400                | pF   |
| t <sub>VD_DAT</sub> | Data valid time <sup>(10)</sup>  |  |                         |     | 0.9 <sup>(4)</sup> | μs   |
| t <sub>VD_ACK</sub> | Data valid acknowledge time <sup>(11)</sup>                                    |  |                         |     | 0.9 <sup>(4)</sup> | μs   |
| V <sub>nL</sub>     | Noise margin at the LOW level  | For each connected device (including hysteresis) | 0.1*AVD<br>D            |     |                    | V    |
| V <sub>nh</sub>     | Noise margin at the HIGH level   | For each connected device (including hysteresis) | 0.2*AVD<br>D            |     |                    | V    |

- (1) All values referred to V<sub>IH(min)</sub> (0.3V<sub>DD</sub>) and V<sub>IL(max)</sub> levels (see Table 9).
- (2) t<sub>HD\_DAT</sub> is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V<sub>IH(min)</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum t<sub>HD\_DAT</sub> could be 3.45 μs and .9 μs for Standard-mode and Fast-mode, but must be less than the maximum of t<sub>VD\_DAT</sub> or t<sub>VD\_ACK</sub> by a transition time. This maximum must only be met if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
- (5) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t<sub>SU\_DAT</sub> 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r(max)</sub> + t<sub>SU\_DAT</sub> = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
- (6) If mixed with Hs-mode devices, faster fall times according to Table 10 are allowed.
- (7) The maximum t<sub>f</sub> for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t<sub>f</sub> is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t<sub>f</sub>.
- (8) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- (9) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
- (10) t<sub>VD\_DAT</sub> = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
- (11) t<sub>VD\_ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

## 6.7 Typical Characteristics

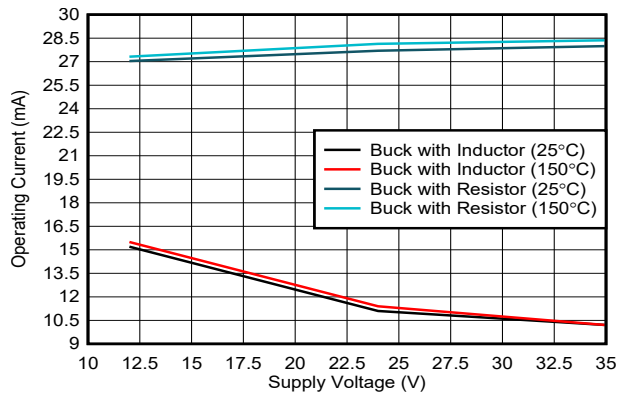


图 6-1. Supply current over supply voltage

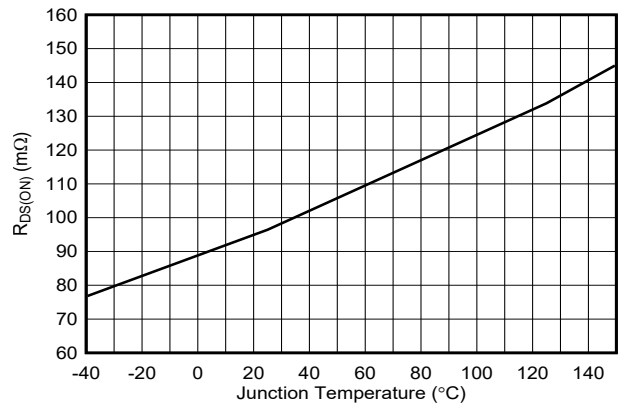


图 6-2.  $R_{DS(ON)}$  (high and low side combined) for MOSFETs over temperature

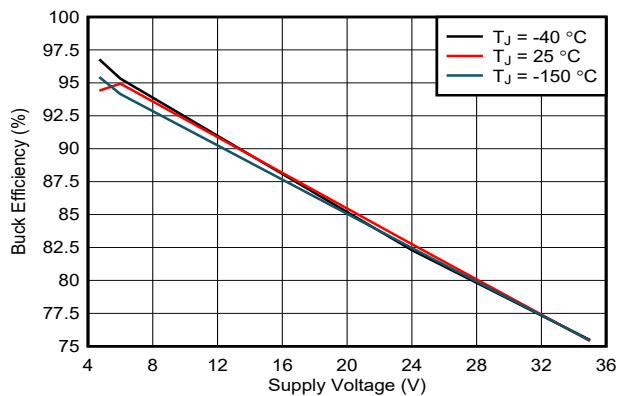


图 6-3. Buck regulator efficiency over supply voltage

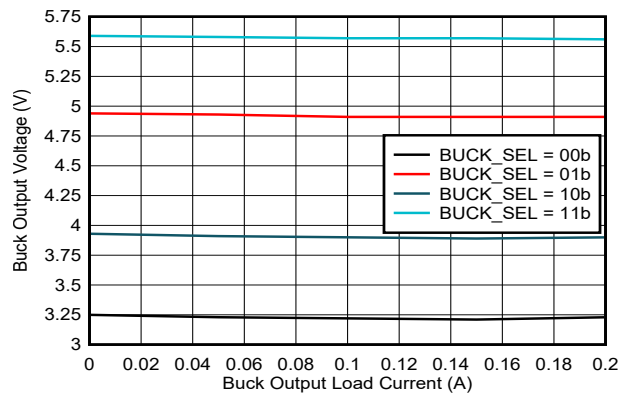


图 6-4. Buck regulator output voltage over load current

## 7 Detailed Description

### 7.1 Overview

The MCF8316A provides a single-chip, code-free sensorless FOC solution for customers driving speed-controlled 12- to 24-V brushless-DC motors requiring up to 8-A peak phase currents.

The MCF8316A integrates three 1/2-H bridges with 40-V absolute maximum capability and a very low  $R_{DS(ON)}$  of 95-m $\Omega$  (high-side + low-side) to enable high power drive capability. Current is sensed using an integrated current sensing circuit which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can be used to power external circuits.

MCF8316A implements Sensorless FOC, and so an external microcontroller is not required to spin the brushless-DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a speed command through a PWM input, analog voltage, frequency input or I<sup>2</sup>C command.

In-built protection features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD\_UV), buck regulator UVLO, motor lock detection and overtemperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the registers.

The MCF8316A device is available in a 0.5-mm pin pitch, VQFN surface-mount package. The VQFN package size is 7 mm × 5 mm with a height of 1 mm.

### 7.2 Functional Block Diagram

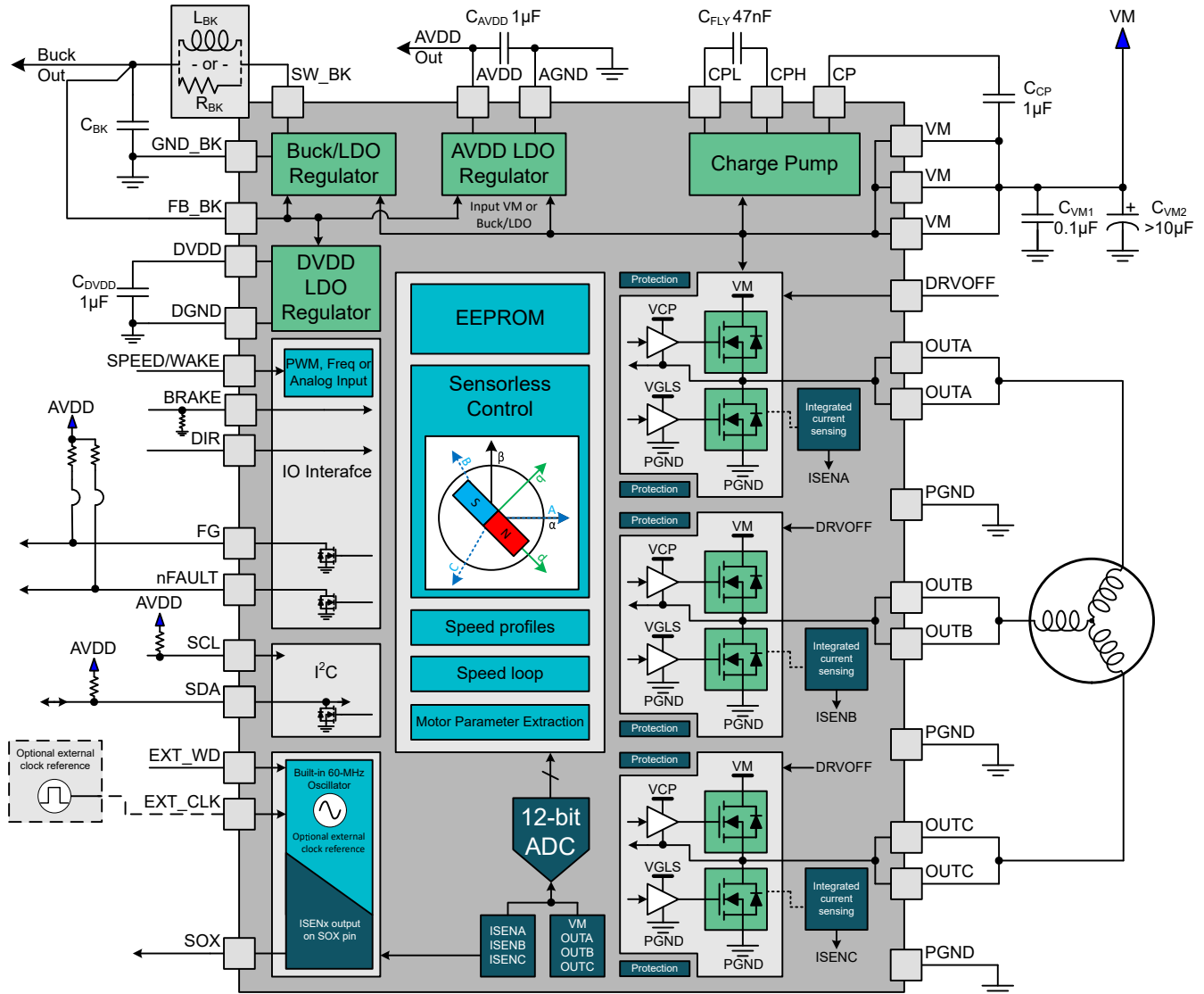


图 7-1. MCF8316A Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Output Stage

The MCF8316A consists of an integrated 95-mΩ (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

### 7.3.2 Device Interface Modes

The MCF8316A supports I<sup>2</sup>C interface to provide end application design with adequate flexibility. MCF8316A allows controlling the motor operation and system through BRAKE, DRVOFF, DIR, EXT\_CLK, EXT\_WD and SPEED/WAKE. MCF8316A also provides different signals for monitoring speed, fault and phase current feedback through FG, nFAULT and SOX .

#### 7.3.2.1 Interface - Control and Monitoring

Motor Control Signals

- When BRAKE pin is driven 'High', MCF8316A enters brake state. Brake state can be configured to either low side braking (see [Low-Side Braking](#)) or align brake (see [Align Braking](#)) through BRAKE\_PIN\_MODE. MCF8316A decreases output speed to value defined by BRAKE\_SPEED\_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCF8316A stays in brake state. Brake pin input can be overwritten by configuring BRAKE\_INPUT over the I<sup>2</sup>C interface.
- The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUT A → OUT B → OUT C, and when driven 'Low' the sequence is OUT A → OUT C → OUT B. DIR pin input can be overwritten by configuring DIR\_INPUT over the I<sup>2</sup>C interface.
- When DRVOFF pin is driven 'High', MCF8316A stops driving the motor by turning OFF all MOSFETs (coast state). When DRVOFF is driven 'Low', MCF8316A returns to normal state of operation, as if it was restarting the motor (see [DRVOFF Functionality](#)). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED pin.
- SPEED/WAKE pin is used to control motor speed and wake up MCF8316A from sleep mode. SPEED pin can be configured to accept PWM, frequency or analog input signals. It is used to enter and exit from sleep and standby mode (see [表 7-6](#)).

External Oscillator and Watchdog Signals (Optional)

- EXT\_CLK pin may be used to provide an external clock reference (see [External Clock Source](#) ).
- EXT\_WD pin may be used to provide an external watchdog signal (see [External Watchdog](#)).

Output Signals

- FG pin provides pulses which are proportional to motor speed (see [FG Configuration](#)).
- nFAULT pin provides fault status in device or motor operation.
- SOX pin provides the output of one of the current sense amplifiers.

#### 7.3.2.2 I<sup>2</sup>C Interface

The MCF8316A supports an I<sup>2</sup>C serial communication interface that allows an external controller to send and receive data. This I<sup>2</sup>C interface lets the external controller configure the EEPROM and read detailed fault and motor state information. The I<sup>2</sup>C bus is a two-wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

### 7.3.3 Step-Down Mixed-Mode Buck Regulator

The MCF8316A has an integrated mixed-mode buck regulator in conjunction with AVDD to supply regulated 3.3 V or 5 V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4 V or 5.7 V for supporting the extra headroom for external LDO for generating a 3.3 V or 5 V supplies. The output voltage of the buck is set by BUCK\_SEL.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

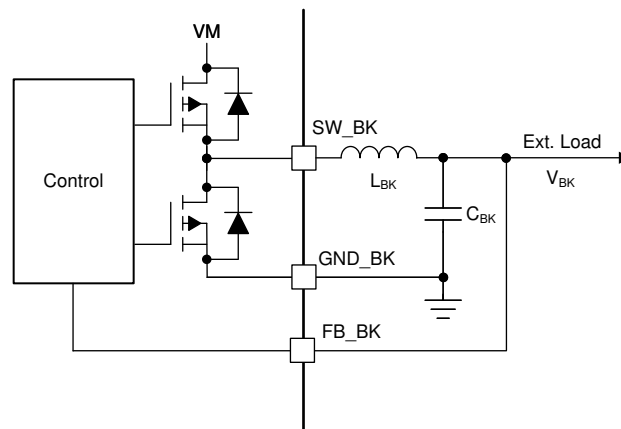
**表 7-1. Recommended settings for Buck Regulator**

| Buck Mode              | Buck output voltage | Max output current from AVDD ( $I_{AVDD\_MAX}$ ) | Max output current from Buck ( $I_{BK\_MAX}$ ) | Buck current limit    | AVDD power sequencing            |
|------------------------|---------------------|--|--|-----------------------|----------------------------------|
| Inductor - 47 $\mu$ H  | 3.3 V or 4 V        | 20 mA  | 170 mA - $I_{AVDD}$                            | 600 mA (BUCK_CL = 0b) | Not supported (BUCK_PS_DIS = 1b) |
| Inductor - 47 $\mu$ H  | 5 V or 5.7 V        | 20 mA  | 170 mA - $I_{AVDD}$                            | 600 mA (BUCK_CL = 0b) | Supported (BUCK_PS_DIS = 0b)     |
| Inductor - 22 $\mu$ H  | 5 V or 5.7 V        | 20 mA  | 20 mA - $I_{AVDD}$                             | 150 mA (BUCK_CL = 1b) | Not supported (BUCK_PS_DIS = 1b) |
| Inductor - 22 $\mu$ H  | 3.3 V or 4 V        | 20 mA  | 20 mA - $I_{AVDD}$                             | 150 mA (BUCK_CL = 1b) | Supported (BUCK_PS_DIS = 0b)     |
| Resistor - 22 $\Omega$ | 5 V or 5.7 V        | 20 mA  | 10 mA - $I_{AVDD}$                             | 150 mA (BUCK_CL = 1b) | Not supported (BUCK_PS_DIS = 1b) |
| Resistor - 22 $\Omega$ | 3.3 V or 4 V        | 20 mA  | 10 mA - $I_{AVDD}$                             | 150 mA (BUCK_CL = 1b) | Supported (BUCK_PS_DIS = 0b)     |

#### 7.3.3.1 Buck in Inductor Mode

The buck regulator in MCF8316A is primarily designed to support low inductance of 47- $\mu$ H and 22- $\mu$ H. A 47- $\mu$ H inductor allows the buck regulator to operate up to 170-mA load current support, whereas applications requiring current up to 20-mA can use a 22- $\mu$ H inductor which saves component size.

图 7-2 shows the connection of buck regulator in inductor mode.



**图 7-2. Buck (Inductor Mode)**

### 7.3.3.2 Buck in Resistor mode

If the external load requirement is less than 10-mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

图 7-3 shows the connection of buck in resistor mode.

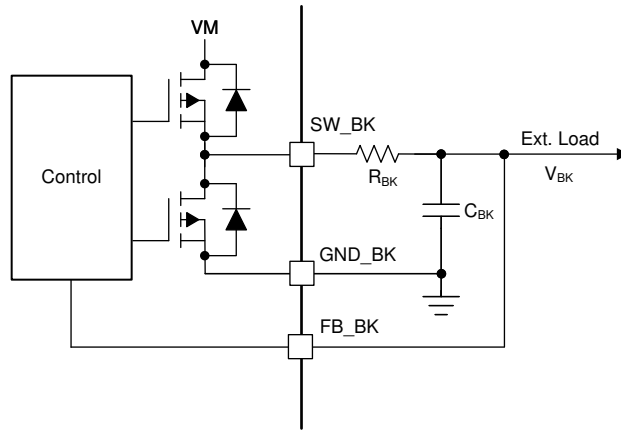


图 7-3. Buck (Resistor Mode)

### 7.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to supply an external LDO to generate standard 3.3-V or 5-V output rail with higher accuracies. The buck output voltage should be configured to 4-V or 5.7-V to provide extra headroom to support the external LDO for generating 3.3-V or 5-V rail as shown in 图 7-4. This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

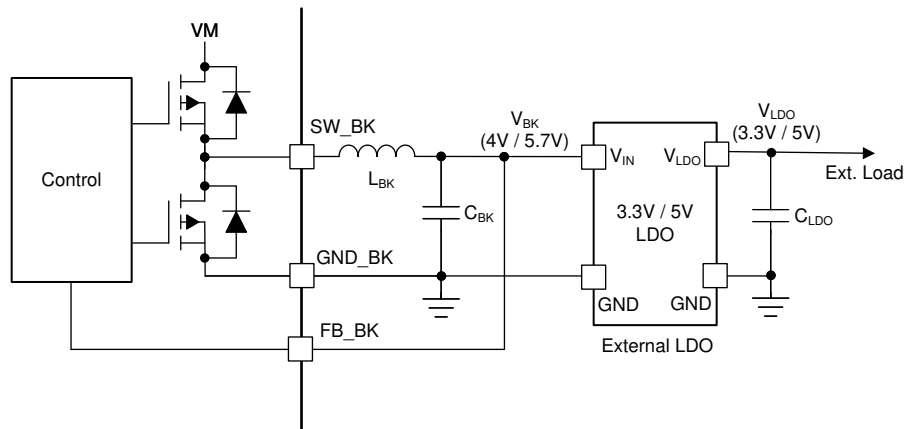


图 7-4. Buck Regulator with External LDO

### 7.3.3.4 AVDD Power Sequencing from Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce the device power dissipation. The power sequencing mode allows on-the-fly changeover of AVDD LDO input from DC mains (VM) to buck output ( $V_{BK}$ ) as shown in 图 7-5. This sequencing can be configured through the BUCK\_PS\_DIS bit . Power sequencing is supported only when buck output voltage is set to 5-V or 5.7-V.

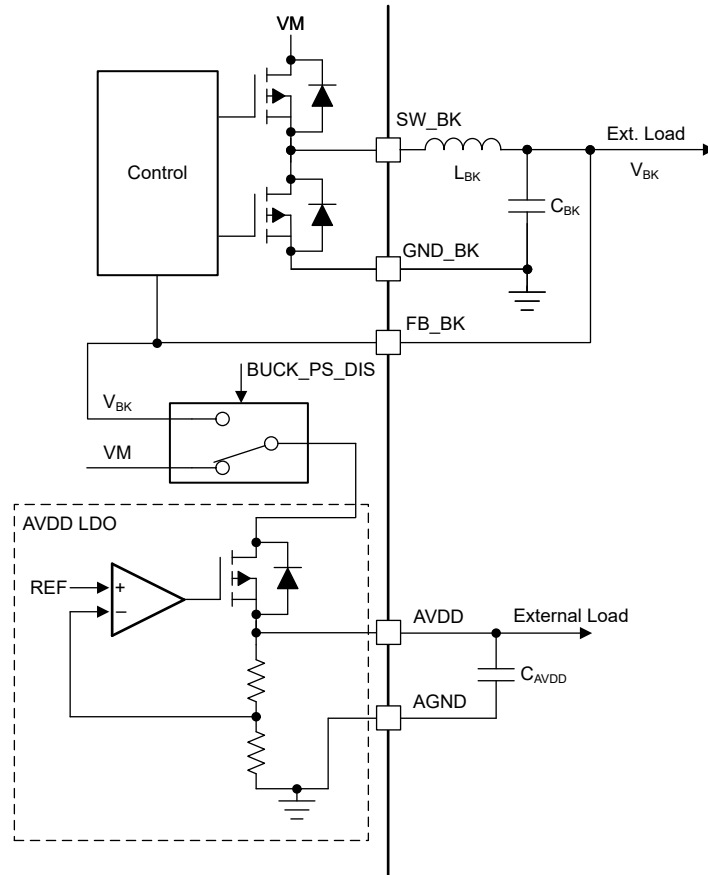
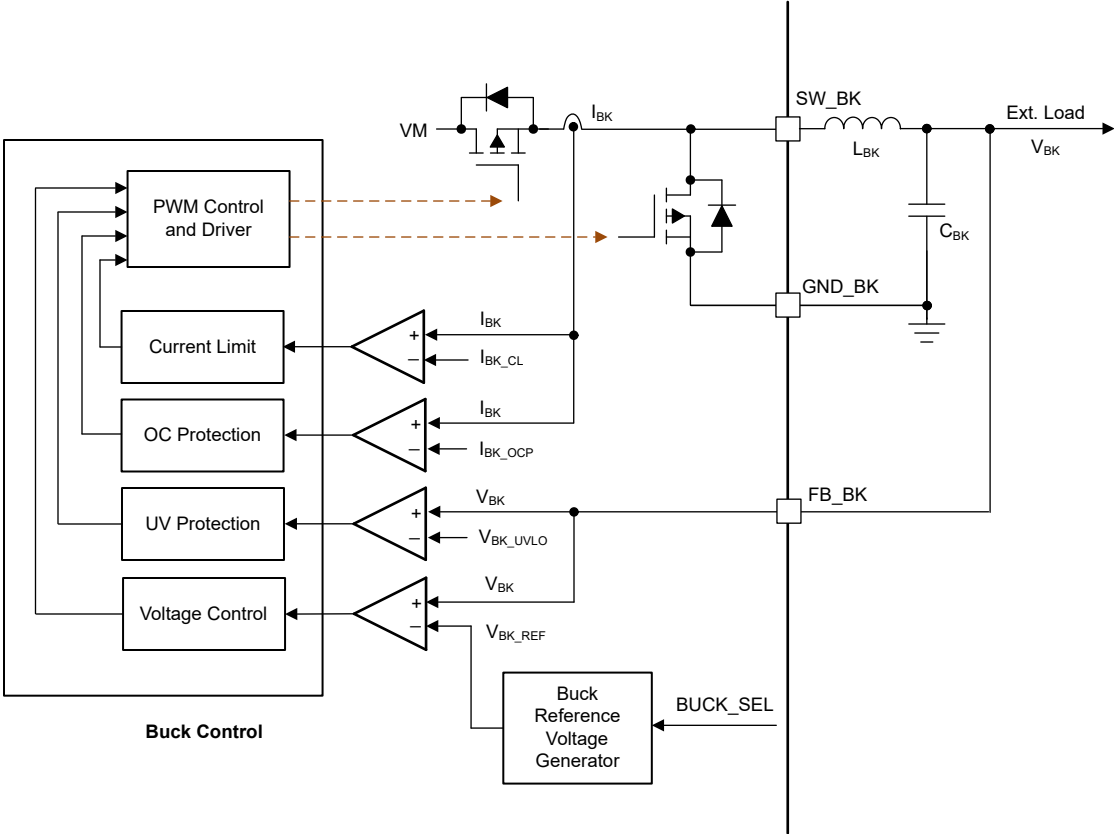
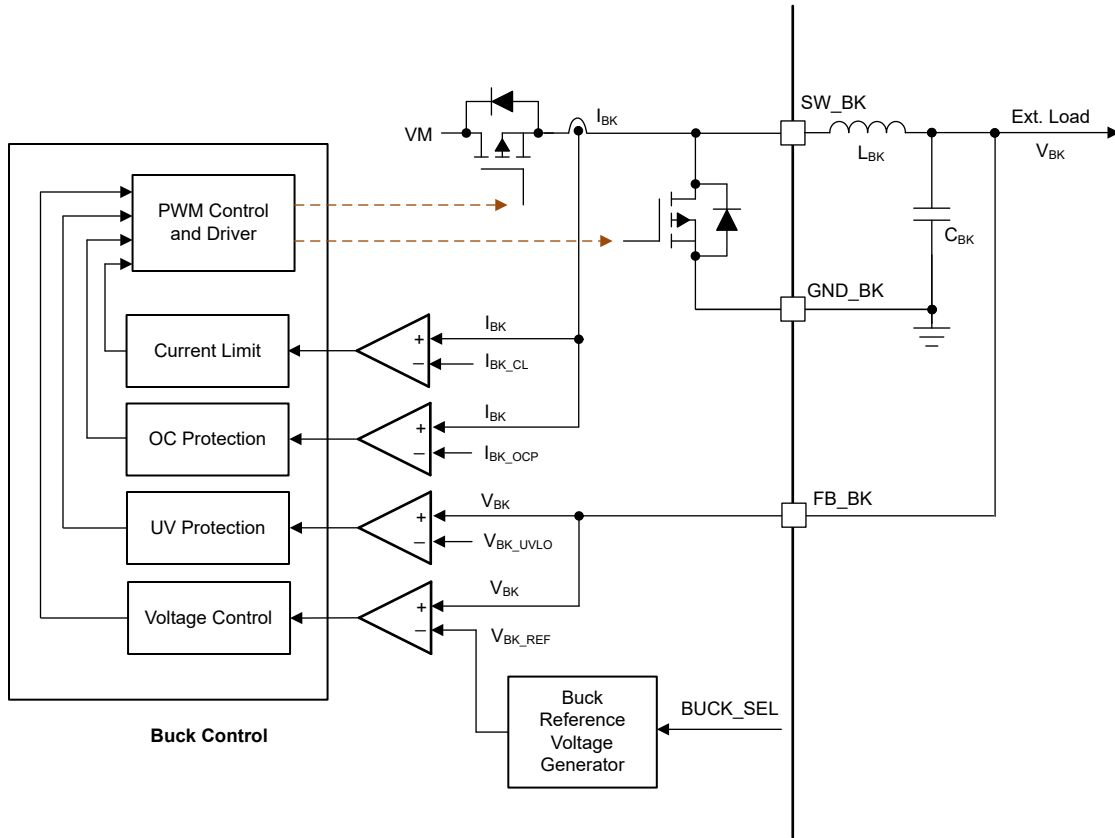


图 7-5. AVDD Power Sequencing from Mixed Mode Buck Regulator

### 7.3.3.5 Mixed Mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage ( $V_{BK\_REF}$ ) which is internally generated depending on the buck-output voltage setting (BUCK\_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ( $V_{BK} < V_{BK\_REF}$ ) or low ( $V_{BK} > V_{BK\_REF}$ ), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in high-side power FET ( $I_{BK}$ ) and turns off the high-side FET when the current becomes higher than the buck current limit ( $I_{BK\_CL}$ ). This implements a current limit control for the buck regulator.  shows the architecture of the buck and various control/protection loops.



**图 7-6. Buck Operation and Control Loops**

### 7.3.3.6 Buck Undervoltage Protection

If at any time the voltage on the FB\_BK pin (buck regulator output) falls lower than the  $V_{BK\_UVLO}$  threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled. MCF8316A goes into reset state whenever buck UV event occurs, since the internal circuitry in MCF8316A is powered from the buck regulator output.

### 7.3.3.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the  $I_{BK\_OCP}$  threshold for a time longer than the deglitch time ( $t_{OCP\_DEG}$ ), a buck OCP event is recognized. MCF8316A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8316A is powered from the buck regulator output.

### 7.3.4 AVDD Linear Voltage Regulator

A 3.3-V, linear regulator is integrated into the MCF8316A and is available for use by external circuitry. The AVDD LDO regulator is used for powering up the internal circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 20-mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1- $\mu$ F, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3-V.

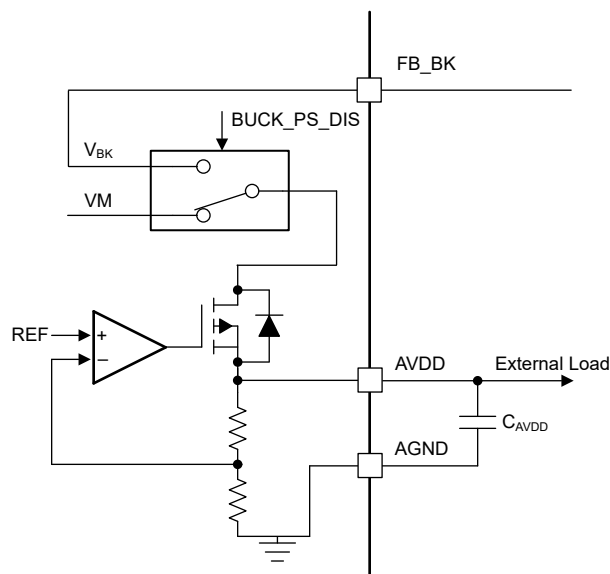


图 7-7. AVDD Linear Regulator Block Diagram

Use [方程式 1](#) to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK\_PS\_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a  $V_{VM}$  of 24-V, drawing 20-mA out of AVDD results in a power dissipation as shown in [方程式 2](#).

$$P = (24 \text{ V} - 3.3 \text{ V}) \times 20 \text{ mA} = 414 \text{ mW} \quad (2)$$

Use [方程式 3](#) to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK\_PS\_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

### 7.3.5 Charge Pump

Since the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to turn-on the high-side FETs. The MCF8316A integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors ( $C_{CP}$ ,  $C_{FLY}$ ) for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

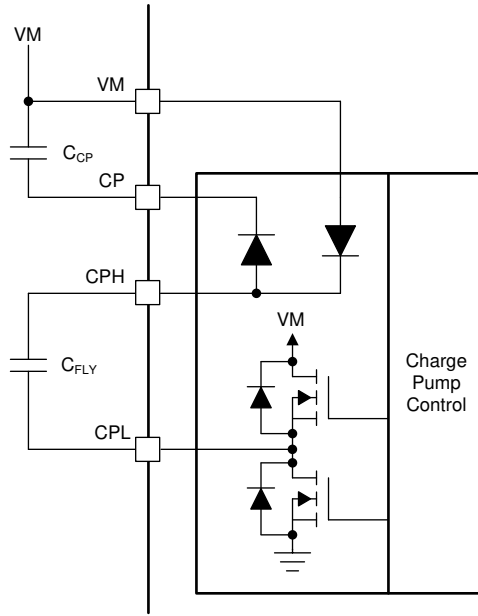
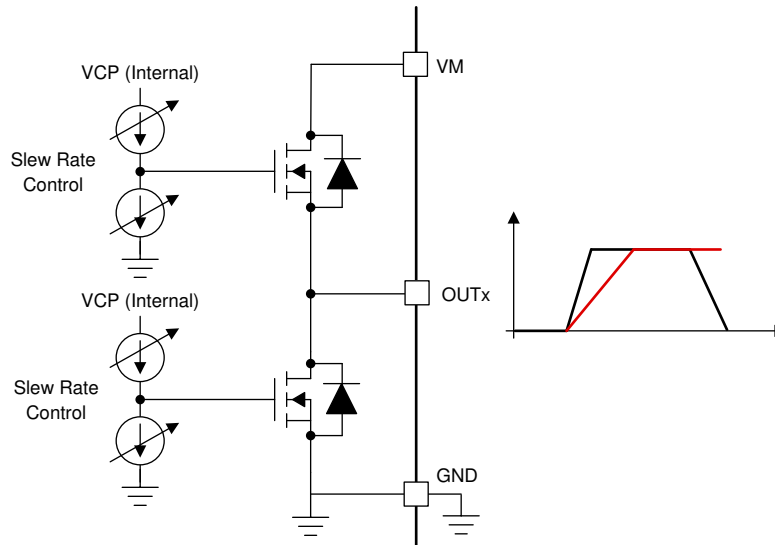


图 7-8. Charge Pump

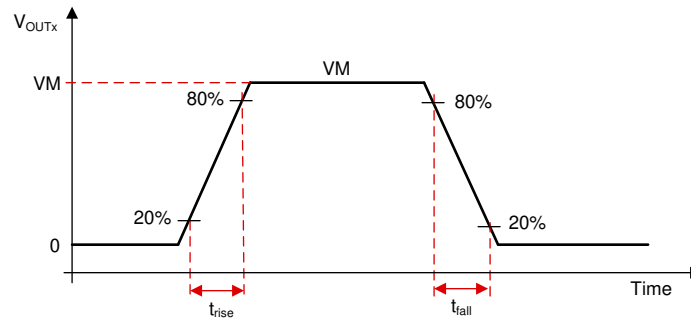
### 7.3.6 Slew Rate Control

An adjustable gate-drive current control for the MOSFETs in the output stage is provided to achieve configurable slew rate for EMI mitigation. The MOSFET VDS slew rate is a critical factor for optimizing radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. This slew rate is predominantly determined by the control of the internal MOSFET gate current as shown in [图 7-9](#).



**图 7-9. Slew Rate Circuit Implementation**

The slew rate of each half-bridge can be adjusted through SLEW\_RATE settings. Slew rate can be configured as 25-V/ $\mu$ s, 50-V/ $\mu$ s, 125-V/ $\mu$ s or 200-V/ $\mu$ s. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in [图 7-10](#).

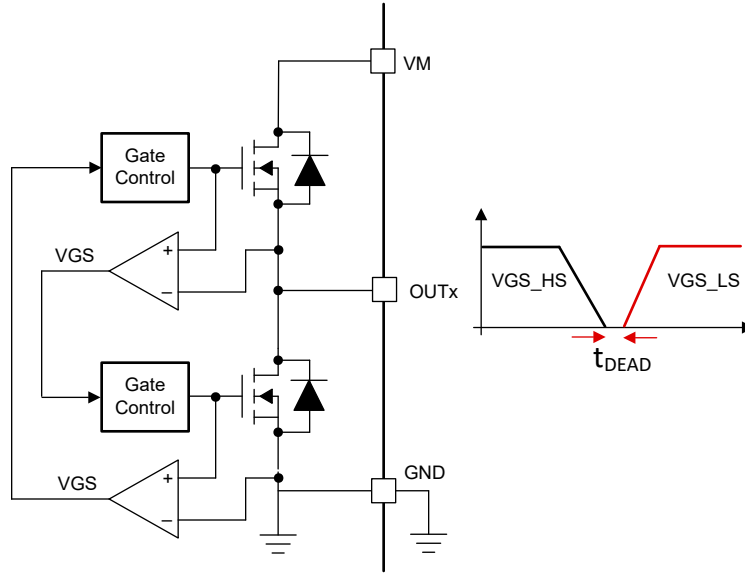


**图 7-10. Slew Rate Timings**

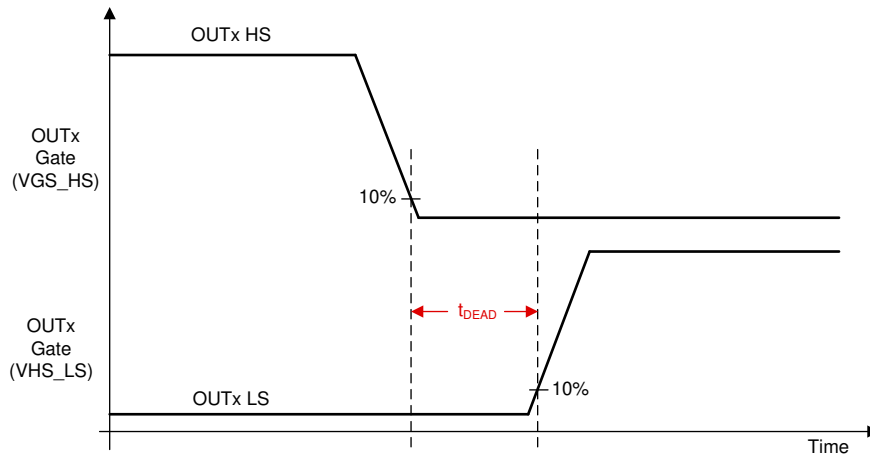


### 7.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of the MOSFETs. The high-side and low-side MOSFETs are carefully controlled to avoid any shoot-through events by inserting a dead time ( $t_{dead}$ ). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that the VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in [图 7-11](#) and [图 7-12](#) and vice versa.



**图 7-11. Cross Conduction Protection**



**图 7-12. Dead Time**

### 7.3.8 SPEED Control

The MCF8316A offers four methods of directly controlling the speed of the motor. The speed control method is configured by SPEED\_MODE. The speed command can be controlled in one of the following four ways.

- PWM input on SPEED pin by varying duty cycle of input signal
- Frequency input on SPEED pin by varying frequency of input signal
- Analog input on SPEED pin by varying amplitude of input signal
- Over I<sup>2</sup>C by configuring DIGITAL\_SPEED\_CTRL register

The speed can also be indirectly controlled by varying the supply voltage ( $V_M$ ).

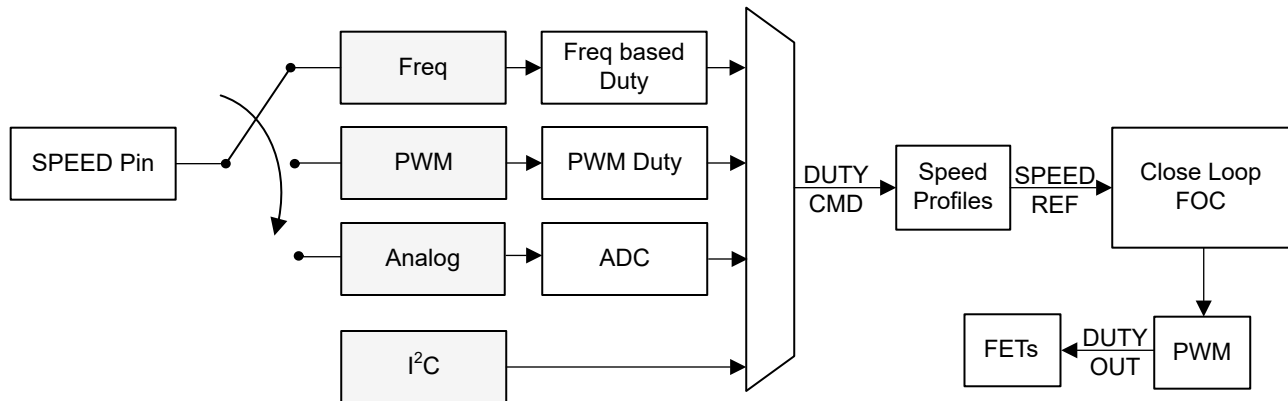


图 7-13. Multiplexing the Speed Command

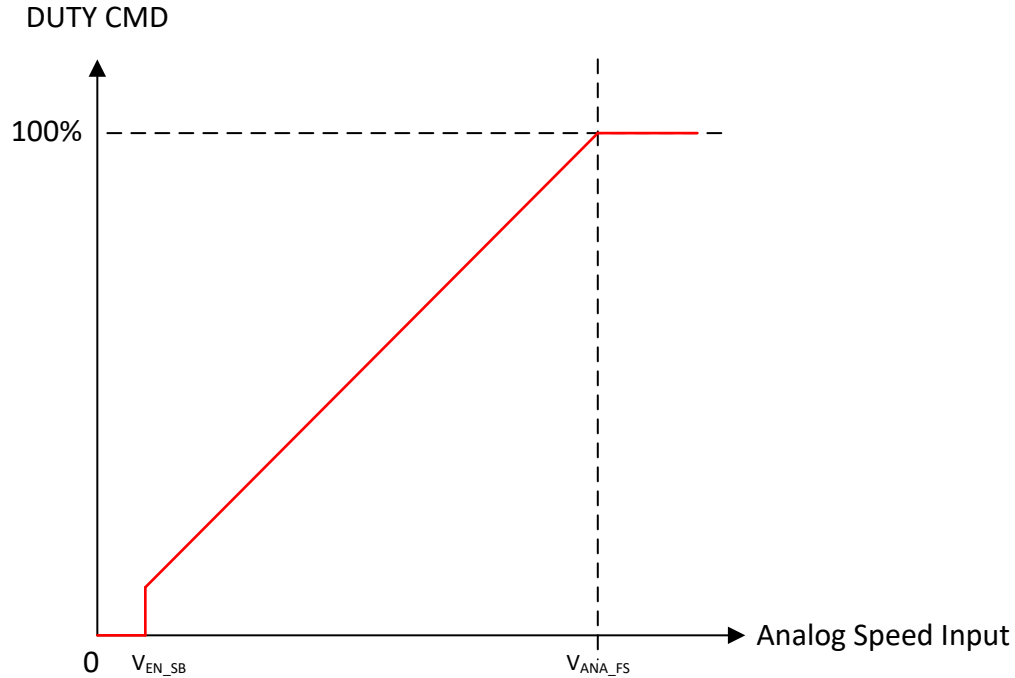
The signal path from SPEED pin input (or I<sup>2</sup>C based speed input) to output duty cycle (DUTY OUT) applied to FETs is shown in 图 7-13.

#### 备注

1. Any duty command (DUTY CMD from SPEED pin or I<sup>2</sup>C) or speed reference (SPEED REF from speed profiles) value set to < 1% will result in speed reference (SPEED REF) being clamped to zero and motor to be in stopped state.
2. If MAX\_SPEED is set to 0, SPEED REF is clamped to zero (irrespective of DUTY CMD) and motor is in stopped state.

#### 7.3.8.1 Analog-Mode Speed Control

Analog input based speed control can be configured by setting SPEED\_MODE to 00b. In this mode, the duty command (DUTY CMD) varies with the analog voltage input on the SPEED pin ( $V_{SPEED}$ ). When  $0 < V_{SPEED} < V_{EN\_SB}$ , DUTY CMD is set to zero and the motor is stopped. When  $V_{EN\_SB} < V_{SPEED} < V_{ANA\_FS}$ , DUTY CMD varies linearly with  $V_{SPEED}$  as shown in 图 7-14. When  $V_{SPEED} > V_{ANA\_FS}$ , DUTY CMD is clamped to 100%.



**图 7-14. Analog-Mode Speed Control**

### 7.3.8.2 PWM-Mode Speed Control

PWM based speed control can be configured by setting SPEED\_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100% and duty command (DUTY CMD) varies linearly with the applied PWM duty cycle. DUTY CMD is set to zero and the motor is stopped when the PWM signal at SPEED pin stays  $< V_{DIG\_IL}$  for longer than  $t_{EN\_SB\_PWM}$ . The frequency of the PWM input signal applied to the SPEED pin is defined as  $f_{PWM}$  and the range for this frequency can be configured through SPEED\_RANGE\_SEL.

#### 备注

$f_{PWM}$  is the frequency of the PWM signal the device can accept at SPEED pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM\_FREQ\_OUT (see [节 7.3.15](#)).

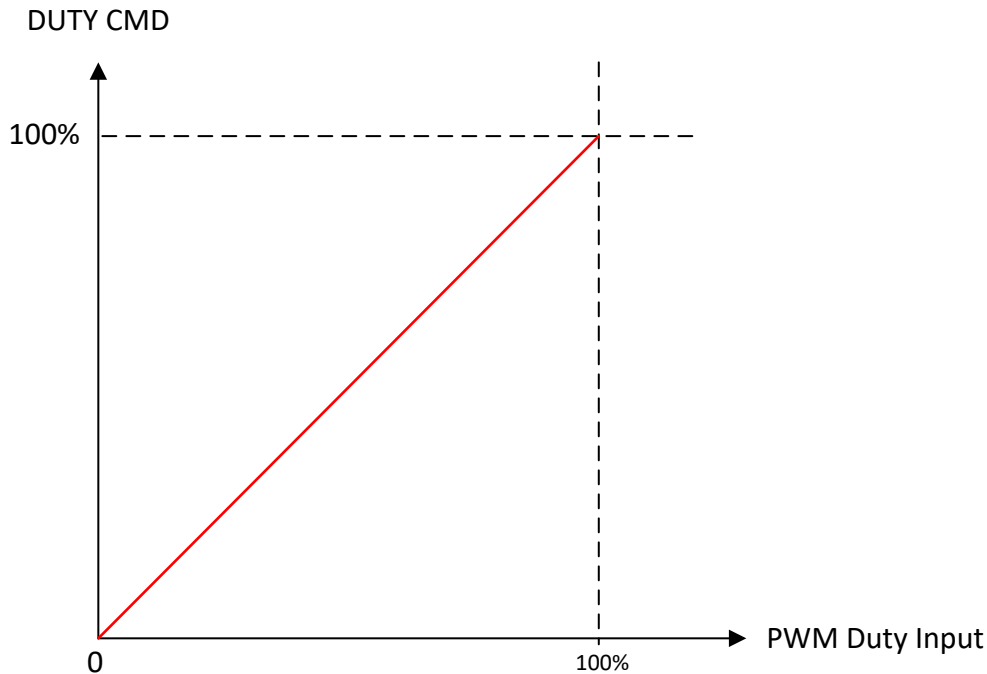


图 7-15. PWM-Mode Speed Control

### 7.3.8.3 I<sup>2</sup>C based Speed Control

I<sup>2</sup>C based serial interface can be used for speed control by setting SPEED\_MODE to 10b. In this mode, the duty command can be written directly into DIGITAL\_SPEED\_CTRL register and the SPEED pin can be independently used to control the sleep entry and exit. If SPEED pin input is  $< V_{EN\_SL}$  for a time longer than SLEEP\_ENTRY\_TIME, MCF8316A enters sleep state irrespective of the I<sup>2</sup>C duty command in DIGITAL\_SPEED\_CTRL register. When SPEED pin  $> V_{EX\_SL}$ , MCF8316A exits sleep state and speed is controlled through DIGITAL\_SPEED\_CTRL register. If DIGITAL\_SPEED\_CTRL register is set to 0 and SPEED pin  $> V_{EX\_SL}$ , MCF8316A is in standby state.

### 7.3.8.4 Frequency-Mode Speed Control

Frequency based speed control is configured by setting SPEED\_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED pin as given in 方程式 4. Input frequency greater than INPUT\_MAXIMUM\_FREQ clamps the duty command to 100%. The duty command is set to zero and the motor is stopped when the frequency signal at SPEED pin stays  $< V_{DIG\_IL}$  for longer than  $t_{EN\_SB\_FREQ}$ .

$$\text{Duty command} = \text{Frequency at SPEED pin} / \text{INPUT\_MAXIMUM\_FREQ} * 100 \quad (4)$$

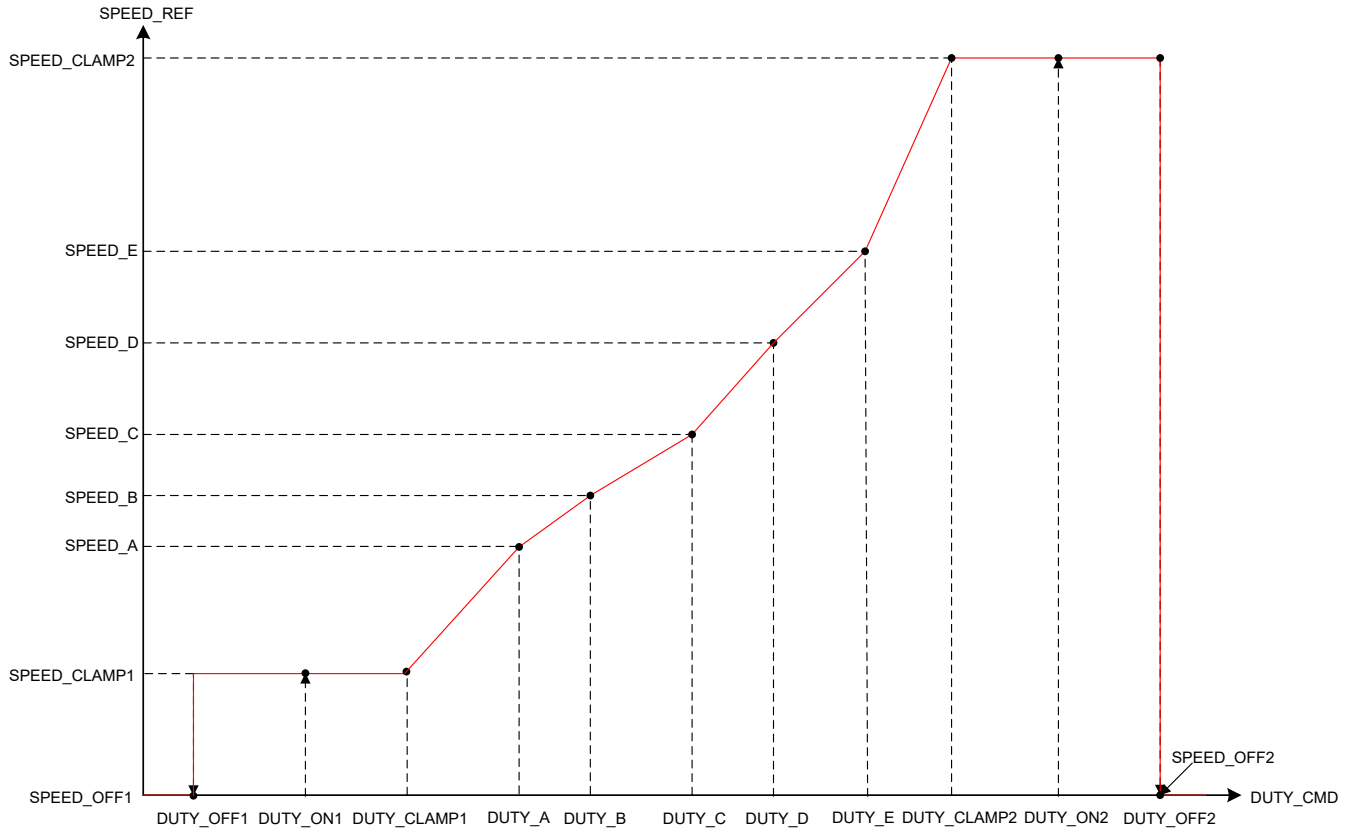
### 7.3.8.5 Speed Profiles

MCF8316A supports three different kinds of speed profiles(linear, step, forward-reverse) to enable a variety of end-user applications. The different speed profiles can be configured through SPEED\_PROFILE\_CONFIG. When SPEED\_PROFILE\_CONFIG is set to 00b, the speed reference is the same as the duty command.

#### 7.3.8.5.1 Linear Speed Profiles

#### 备注

For all types of speed profiles, duty command = 0 stops the motor irrespective of the speed profile register settings.



**图 7-16. Linear Speed Profiles**

Linear speed profiles can be configured by setting SPEED\_PROFILE\_CONFIG to 01b. Linear speed profiles feature speed references which change linearly between SPEED\_CLAMP1 and SPEED\_CLAMP2 with different slopes which can be set by configuring DUTY\_x and SPEED\_x combination.

- DUTY\_ON1 configures the duty command above which MCF8316A starts driving the motor (to speed reference set by SPEED\_CLAMP1) when the current speed reference is zero. When current speed reference is zero and duty command is below DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.
- DUTY\_OFF1 configures the duty command below which the speed reference changes to SPEED\_OFF1, if SPEED\_OFF1 > SPEED\_CLAMP1. If SPEED\_OFF1 < SPEED\_CLAMP1, speed reference is set to SPEED\_CLAMP1.
- DUTY\_CLAMP1 configures the duty command till which speed reference will be constant. SPEED\_CLAMP1 configures this constant speed reference between between DUTY\_OFF1 and DUTY\_CLAMP1.
- DUTY\_A configures the duty command for speed reference SPEED\_A. The speed reference changes linearly between DUTY\_CLAMP1 and DUTY\_A.
- DUTY\_B configures the duty command for speed reference SPEED\_B. The speed reference changes linearly between DUTY\_A and DUTY\_B.
- DUTY\_C configures the duty command for speed reference SPEED\_C. The speed reference changes linearly between DUTY\_B and DUTY\_C.
- DUTY\_D configures the duty command for speed reference SPEED\_D. The speed reference changes linearly between DUTY\_C and DUTY\_D.
- DUTY\_E configures the duty command for speed reference SPEED\_E. The speed reference changes linearly between DUTY\_D and DUTY\_E.
- DUTY\_CLAMP2 configures the duty command above which the speed reference will be constant at SPEED\_CLAMP2. SPEED\_CLAMP2 configures this constant speed reference between DUTY\_CLAMP2 and DUTY\_OFF2. The speed reference changes linearly between DUTY\_E and DUTY\_CLAMP2.

- DUTY\_ON2 configures the duty command below which MCF8316A starts driving the motor (to speed reference set by SPEED\_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.
- DUTY\_OFF2 configures the duty command above which the speed reference will change from SPEED\_CLAMP2 to SPEED\_OFF2.

### 7.3.8.5.2 Staircase Speed Profiles

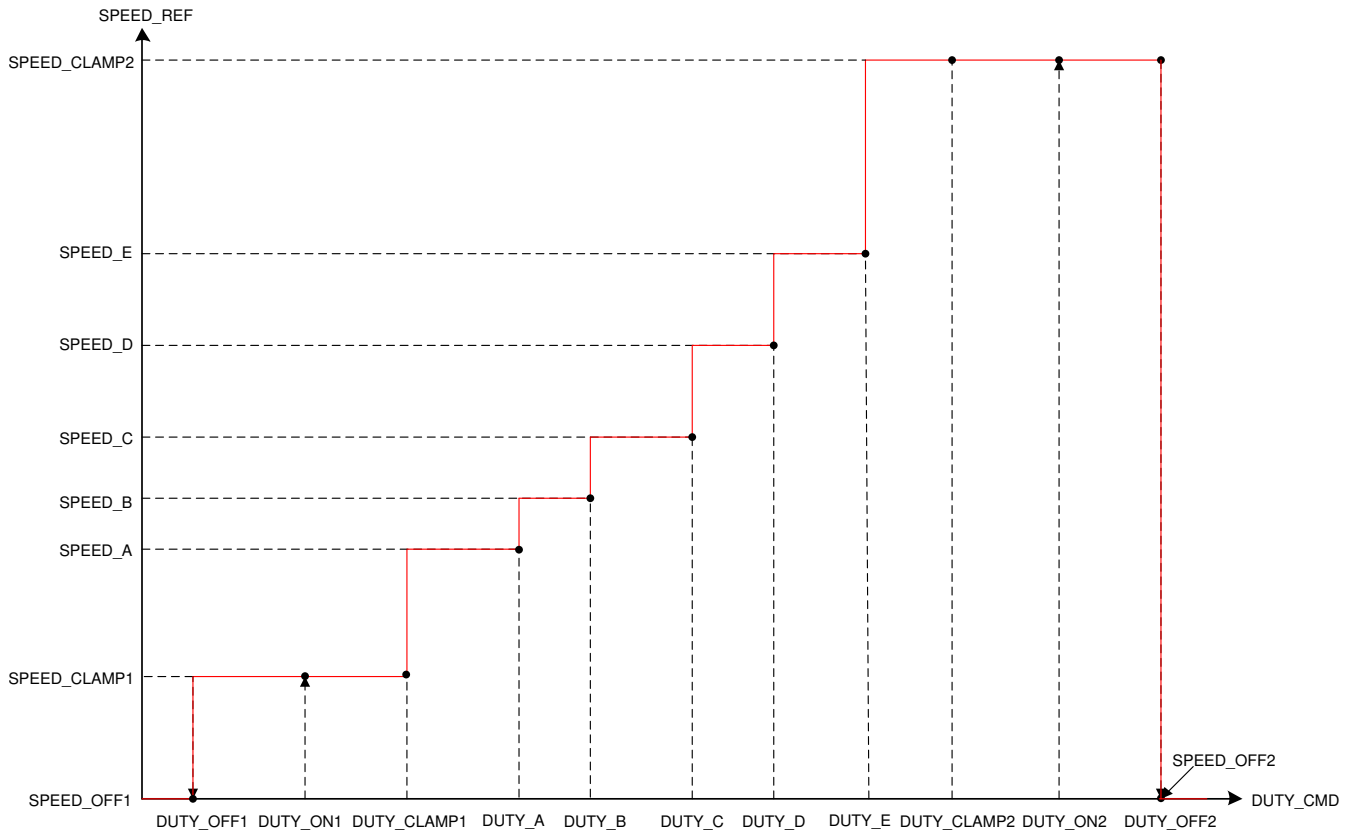


图 7-17. Staircase Speed Profiles

Staircase speed profiles can be configured by setting SPEED\_PROFILE\_CONFIG to b10. Staircase speed profiles feature speed changes in steps between SPEED\_CLAMP1 and SPEED\_CLAMP2. DUTY\_x and SPEED\_x configures the speed and duty command at which the step is increased

- DUTY\_ON1 configures the duty command above which MCF8316A starts driving the motor (to speed reference set by SPEED\_CLAMP1) when the current speed reference is zero. When current speed reference is zero and duty command is below DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.
- DUTY\_OFF1 configures the duty command below which the speed reference changes from SPEED\_CLAMP1 to SPEED\_OFF1, if SPEED\_OFF1 > SPEED\_CLAMP1. If SPEED\_OFF1 < SPEED\_CLAMP1, speed reference is set to SPEED\_CLAMP1.
- DUTY\_CLAMP1 configures the duty command till which speed reference will be constant. SPEED\_CLAMP1 configures this constant speed reference between DUTY\_OFF1 and DUTY\_CLAMP1.
- DUTY\_A configures the duty command for speed reference SPEED\_A. There is a step change in speed reference from SPEED\_CLAMP1 to SPEED\_A at DUTY\_CLAMP1.
- DUTY\_B configures the duty command for speed reference SPEED\_B. There is a step change in speed reference from SPEED\_A to SPEED\_B at DUTY\_A.
- DUTY\_C configures the duty command for speed reference SPEED\_C. There is a step change in speed reference from SPEED\_B to SPEED\_C at DUTY\_B.

- DUTY\_D configures the duty command for speed reference SPEED\_D. There is a step change in speed reference from SPEED\_C to SPEED\_D at DUTY\_C.
- DUTY\_E configures the duty command for speed reference SPEED\_E. There is a step change in speed reference from SPEED\_D to SPEED\_E at DUTY\_D.
- DUTY\_CLAMP2 configures the duty command above which the speed reference will be constant at SPEED\_CLAMP2. SPEED\_CLAMP2 configures this constant speed reference between DUTY\_CLAMP2 and DUTY\_OFF2. There is a step change in speed reference from SPEED\_E to SPEED\_CLAMP2 at DUTY\_E.
- DUTY\_ON2 configures the duty command below which MCF8316A starts driving the motor (to speed reference set by SPEED\_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.
- DUTY\_OFF2 configures the duty command above which the speed reference will change from SPEED\_CLAMP2 to SPEED\_OFF2.

### 7.3.8.5.3 Forward-Reverse Speed Profiles

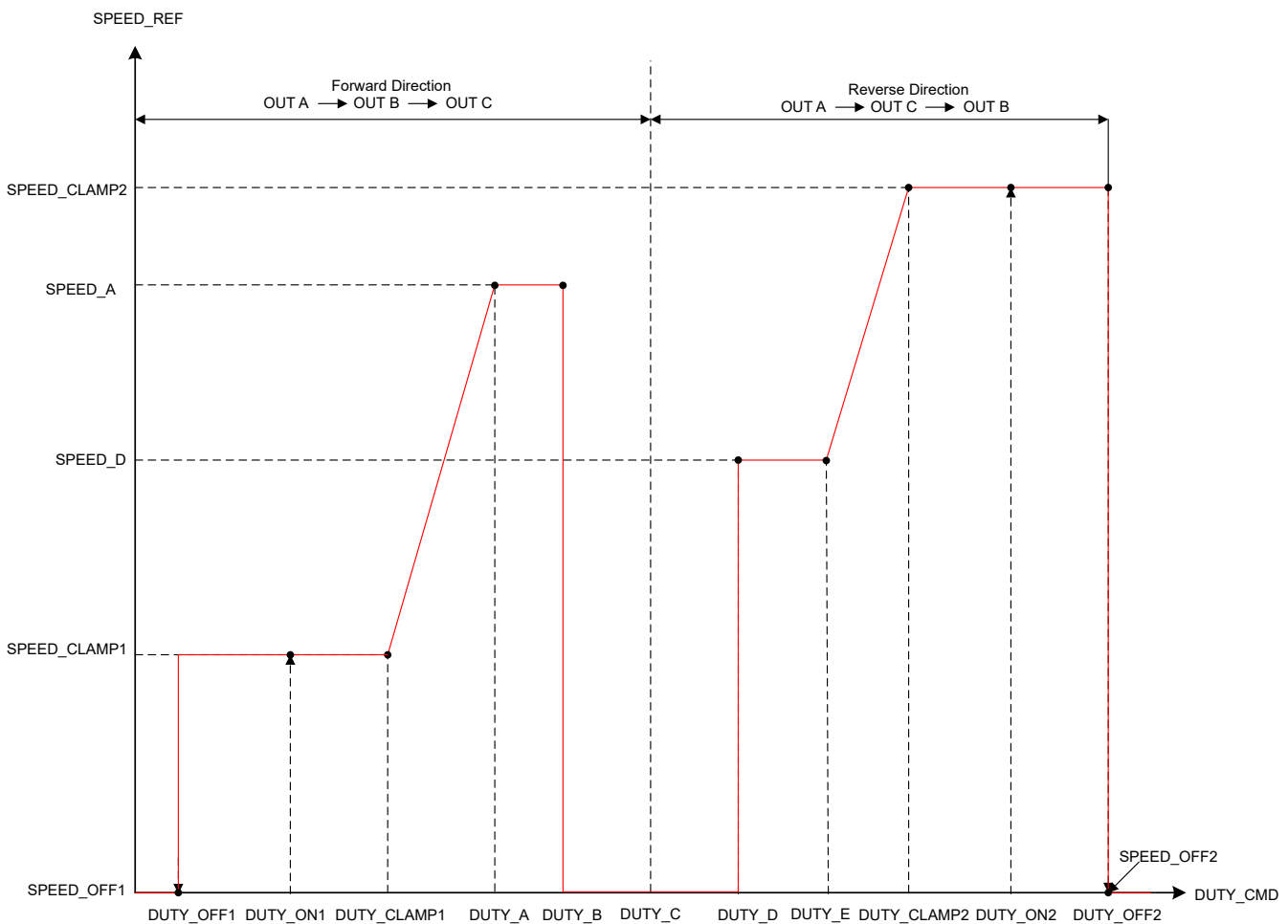


图 7-18. Forward Reverse Speed Profiles

Forward-Reverse speed profiles can be configured by setting SPEED\_PROFILE\_CONFIG to b11. Forward-Reverse speed profiles feature direction change through adjusting the duty command. DUTY\_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

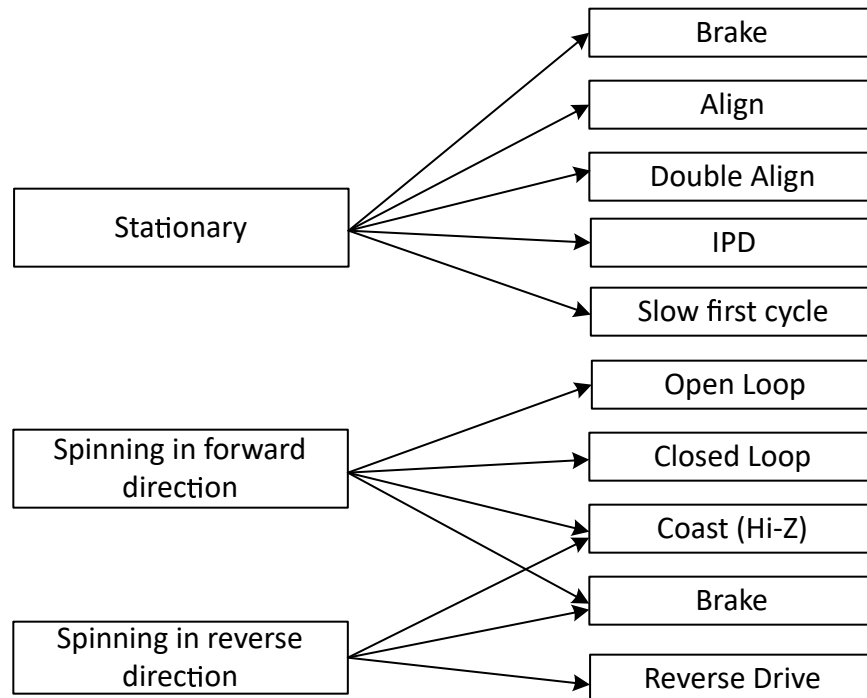
- DUTY\_ON1 configures the duty command above which MCF8316A starts driving the motor in the forward direction (to speed reference set by SPEED\_CLAMP1) when the current speed reference is zero. When

current speed reference is zero and duty command is below DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.

- DUTY\_OFF1 configures the duty command below which the speed reference changes in the forward direction from SPEED\_CLAMP1 to SPEED\_OFF1, if SPEED\_OFF1 > SPEED\_CLAMP1. If SPEED\_OFF1 < SPEED\_CLAMP1, speed reference is set to SPEED\_CLAMP1.
- DUTY\_CLAMP1 configures the duty command at which speed reference will be the constant in forward direction. SPEED\_CLAMP1 configures constant speed reference between DUTY\_CLAMP1 and DUTY\_OFF1.
- DUTY\_A configures the duty command for speed reference SPEED\_A. The speed reference changes linearly between DUTY\_CLAMP1 and DUTY\_A.
- DUTY\_B configures the duty command above which MCF8316A will be in off state. The speed reference remains constant at SPEED\_A between DUTY\_A and DUTY\_B.
- DUTY\_C configures the duty command at which the direction is changed
- DUTY\_D configures the duty command above which the MCF8316A will be in running state in the reverse direction. SPEED\_D configures constant speed reference between DUTY\_D and DUTY\_E.
- DUTY\_CLAMP2 configures the duty command above which speed reference will be constant at SPEED\_CLAMP2 in reverse direction. The speed reference changes linearly between DUTY\_E and DUTY\_CLAMP2.
- DUTY\_ON2 configures the duty command below which MCF8316A starts driving the motor in the reverse direction (to speed reference set by SPEED\_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY\_ON1, MCF8316A continues to be in off state and motor is stationary.
- DUTY\_OFF2 configures the duty command above which the speed reference changes in the reverse direction from SPEED\_CLAMP2 to SPEED\_OFF2.

### 7.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8316A begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8316A includes a number of features to allow for reliable motor start-up under all of these conditions. [图 7-19](#) shows the motor start-up flow for each of the three initial motor states.



**图 7-19. Starting the motor under different initial conditions**



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**备注**

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

---

**7.3.9.1 Case 1 – Motor is Stationary**

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8316A provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8316A also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

**7.3.9.2 Case 2 – Motor is Spinning in the Forward Direction**

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8316A resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8316A enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC\_EN. If resynchronization is disabled, the MCF8316A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

**7.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction**

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8316A provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8316A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

---

**备注**

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

---

### 7.3.10 Motor Start Sequence (MSS)

Figure 7-20 shows the motor-start sequence implemented in the MCF8316A device.

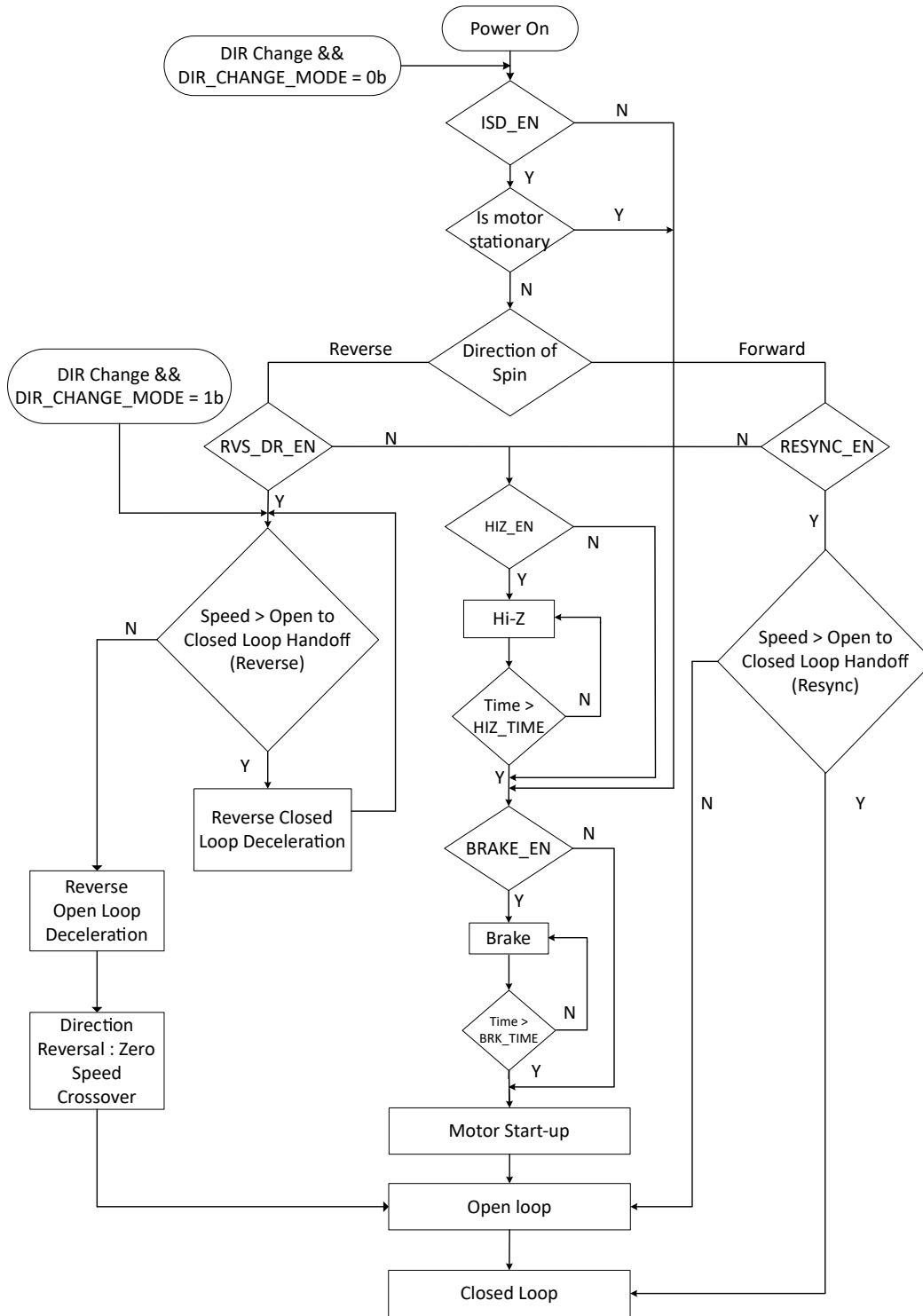


Figure 7-20. Motor Starting-up Flow

#### Power-On State

This is the initial state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCF8316A device comes out of standby or sleep mode.

|   |  |
|---|--|
| <b>DIR Change &amp;&amp;<br/>DIR_CHANGE_MODE = 0b<br/>Judgement</b>                 | In MCF8316A, if direction change command is detected and DIR_CHANGE_MODE is set to 0b during any state (including closed loop), the device re-starts the MSS.  |
| <b>ISD_EN Judgement</b>   | After power-on, the MCF8316A MSS enters the ISD_EN judgement where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement. If ISD is enabled, MSS advances to the ISD (Is Motor Stationary) state.  |
| <b>ISD State</b>  | The MSS determines the initial condition (speed, direction of spin) of the motor (see <a href="#">Initial Speed Detect (ISD)</a> ). If motor is deemed to be stationary (motor BEMF < STAT_DETECT_THR), the MSS proceeds to BRAKE_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.  |
| <b>Direction of Spin<br/>Judgement</b>  | The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8316A proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.   |
| <b>RESYNC_EN Judgement</b>  | If RESYNC_EN is set to 1b, MCF8316A proceeds to Speed > Open to Closed Loop Handoff (Resync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.   |
| <b>Speed &gt; Open to Closed<br/>Loop Handoff (Resync)<br/>Judgement</b>            | If motor speed > OPN_CL_HANDOFF_THR, MCF8316A uses the speed and position information from the ISD state to transition to the closed loop state (see <a href="#">Motor Resynchronization</a> ) directly. If motor speed < OPN_CL_HANDOFF_THR, MCF8316A transitions to open loop state.   |
| <b>RVS_DR_EN Judgement</b>  | The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the HIZ_EN judgement.  |
| <b>Speed &gt; Open to Closed<br/>Loop Handoff (Reverse)<br/>Judgement</b>           | The MSS checks to see if the reverse speed is high enough for MCF8316A to decelerate in closed loop. Till the speed (in reverse direction) is high enough, MSS stays in reverse closed loop deceleration. If speed is too low, then the MSS transitions to reverse open loop deceleration.   |
| <b>Reverse Closed Loop,<br/>Open Loop Deceleration<br/>and Zero Speed Crossover</b> | The MCF8316A resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see <a href="#">Reverse Drive</a> ). When motor speed in reverse direction is too low, the MCF8316A switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high. |
| <b>HIZ_EN Judgement</b>   | The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine. If the coast function is disabled, the MSS advances to the BRAKE_EN judgement.  |
| <b>Coast (Hi-Z) Routine</b>   | The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.  |
| <b>BRAKE_EN Judgement</b>   | The MSS checks to determine whether the brake function is enabled (BRAKE_EN =1). If the brake function is enabled, the MSS advances to the brake routine. If the brake function is disabled, the MSS advances to the motor start-up state (see <a href="#">节 7.3.10.4</a> ).   |
| <b>Brake Routine</b>  | MCF8316A implements a brake by turning on all three (high-side or low-side) MOSFETS for BRK_TIME. Brake is applied either using high-side or low-side MOSFETs based on BRK_MODE configuration.   |
| <b>Closed Loop State</b>  | In this state, the MCF8316A drives the motor with FOC.   |

### 7.3.10.1 Initial Speed Detect (ISD)

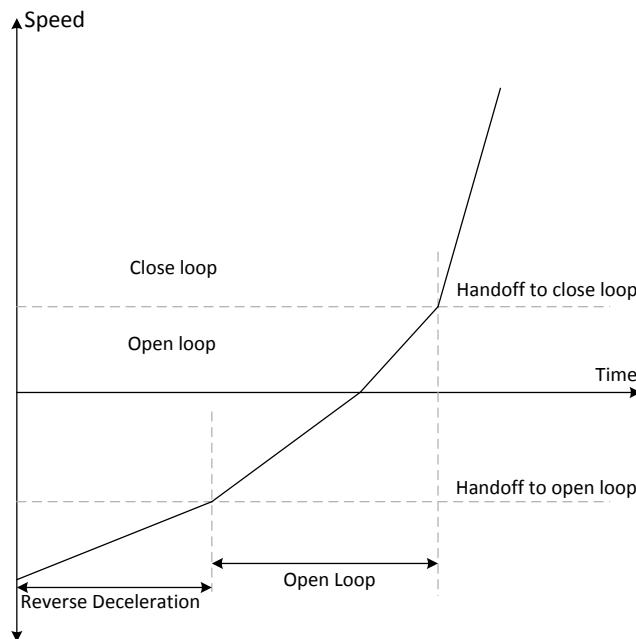
The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD\_EN to 1b. The initial speed, position and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled by setting ISD\_EN to 0b. If the function is disabled (ISD\_EN set to 0b), the MCF8316A does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE\_EN) is enabled.

### 7.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8316A, which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8316A, motor resynchronization can be enabled/disabled through RESYNC\_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

### 7.3.10.3 Reverse Drive

The MCF8316A uses the reverse drive function to change the direction of the motor rotation when ISD\_EN and RVS\_DR\_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see [图 7-21](#)). MCF8316A provides the option of using the forward direction parameters or a separate set of reverse drive parameters by configuring REV\_DRV\_CONFIG.



**图 7-21. Reverse Drive Function**

#### 7.3.10.3.1 Reverse Drive Tuning

MCF8316A provides the option of tuning the open to closed loop handoff threshold, open loop acceleration (and deceleration) rates and open loop current limit in reverse drive to values different to those used in forward drive operation; the reverse drive specific parameters can be used by setting REV\_DRV\_CONFIG to 1b. If REV\_DRV\_CONFIG is set to 0b, MCF8316A uses the equivalent parameters configured for forward drive operation during the reverse drive operation too.

The speed at which motor would enter the open loop in reverse direction can be configured using REV\_DRV\_HANDOFF\_THR. For a smooth transition without jerks or loss of synchronism, user can

configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV\_DRV\_OPEN\_LOOP\_CURRENT. The open loop acceleration rates for the forward direction during speed reversal are defined using REV\_DRV\_OPEN\_LOOP\_ACCEL\_A1 and REV\_DRV\_OPEN\_LOOP\_ACCEL\_A2. The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV\_DRV\_OPEN\_LOOP\_DEC.

#### **7.3.10.4 Motor Start-up**

There are different options available for motor start-up from a stationary position and these options can be configured by MTR\_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

##### **7.3.10.4.1 Align**

Align is enabled by configuring MTR\_STARTUP to 00b. The MCF8316A aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN\_TIME. The phase pattern during align is generated based on ALIGN\_ANGLE. In the MCF8316A, the current limit during align is configured through ALIGN\_OR\_SLOW\_CURRENT LIMIT.

A fast change in the phase current may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCF8316A ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN\_SLOW\_RAMP\_RATE. At the end of align routine the motor, will be aligned at the known position.

##### **7.3.10.4.2 Double Align**

Double align is enabled by configuring MTR\_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180° out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCF8316A provides the option of double align start-up. In double align start-up, MCF8316A uses a phase pattern for the second align that is 90° ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

##### **7.3.10.4.3 Initial Position Detection (IPD)**

Initial Position Detection (IPD) can be enabled by configuring MTR\_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

###### **7.3.10.4.3.1 IPD Operation**

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see [Figure 7-22](#)). When the current reaches the threshold configured by IPD\_CURR\_THR, the MCF8316A stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD\_CURR\_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

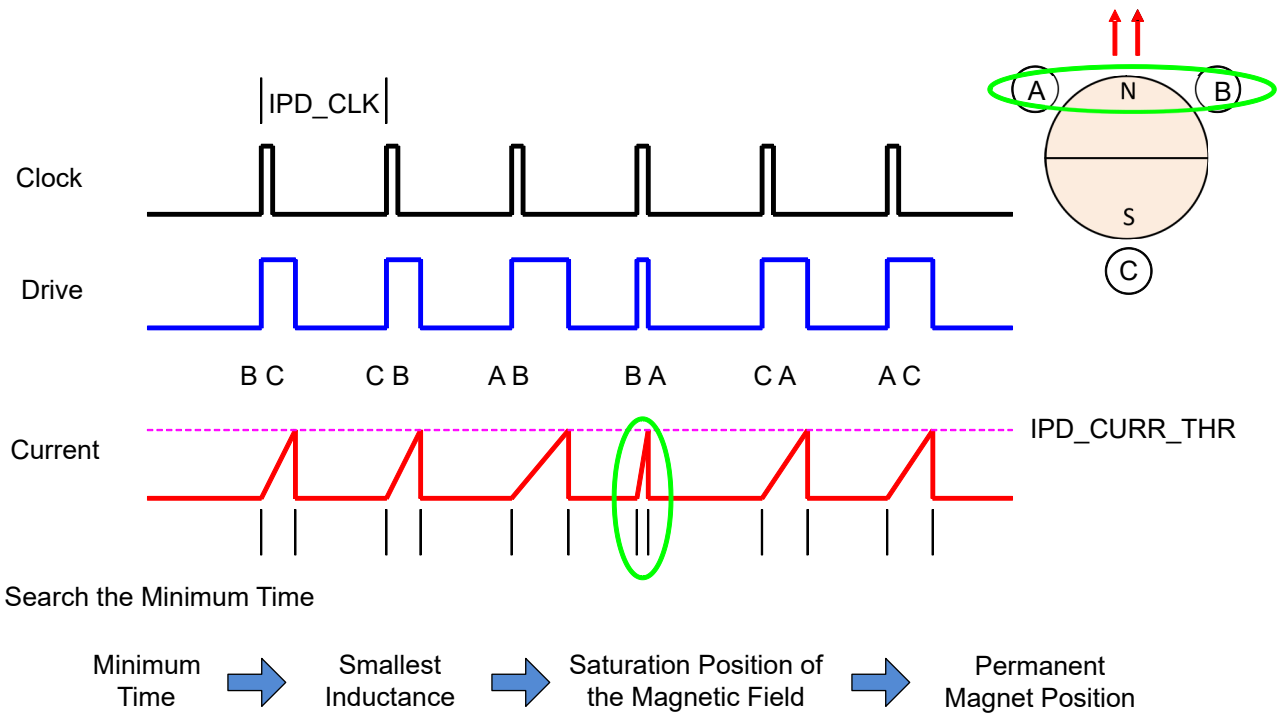


图 7-22. IPD Function

7.3.10.4.3.2 IPD Release Mode

Two modes are available for configuring the way the MCF8316A stops driving the motor when the current threshold is reached. The recirculate (or brake) mode is selected if IPD\_RLS\_MODE = 0b. In this configuration, the low-side (LSC) MOSFET remains ON to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see 图 7-23). Hi-Z mode is selected if IPD\_RLS\_MODE = 1b. In Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see 图 7-24).

In the Hi-Z mode, the phase current has a faster settle-down time, but that can result in a voltage increase on  $V_M$ . The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between  $V_M$  and GND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, recirculate mode must be used. When using the recirculate mode, select the IPD\_CLK\_FREQ appropriately to give the current in the motor windings enough time to decay to 0-A before the next IPD phase pattern is applied.

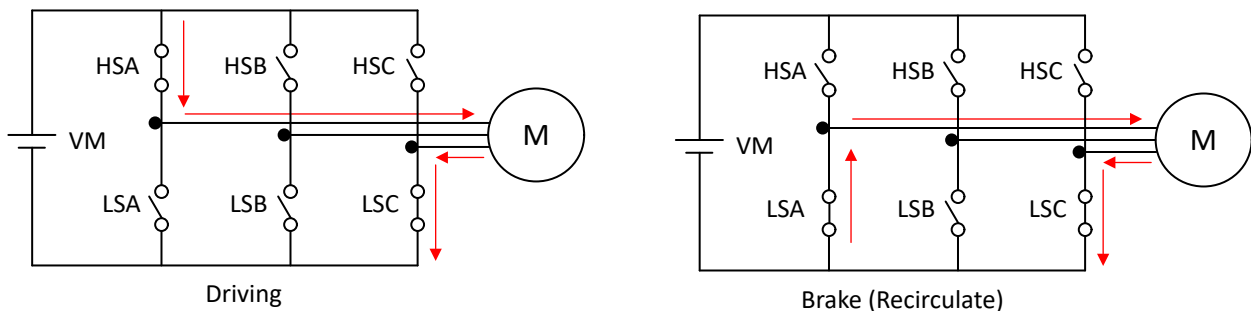


图 7-23. IPD Release Mode 0

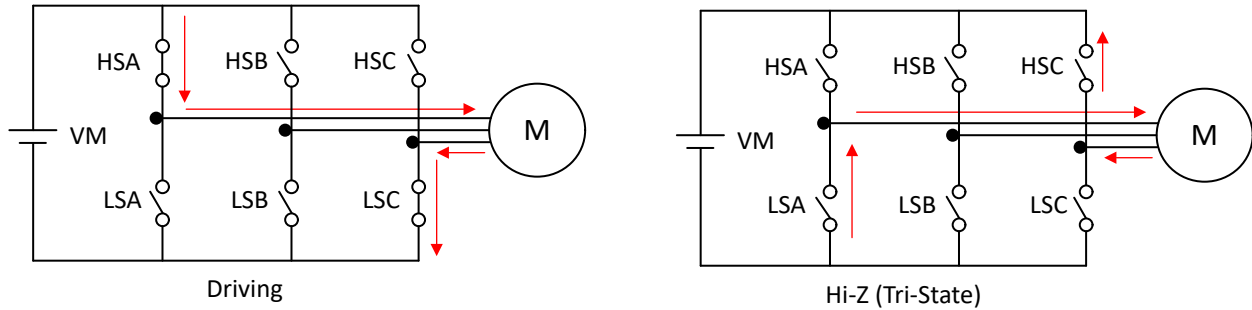


图 7-24. IPD Release Mode 1

#### 7.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8316A begins driving the motor in open loop at an angle specified by IPD\_ADV\_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD\_ADV\_ANGLE to allow for smooth acceleration in the application (see 图 7-25).

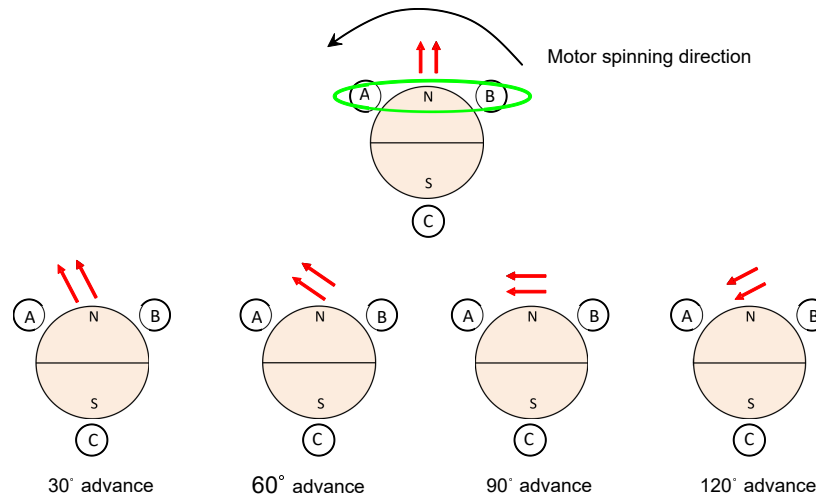


图 7-25. IPD Advance Angle

#### 7.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR\_STARTUP to 11b. In slow first cycle start-up, the MCF8316A starts motor commutation at a frequency defined by SLOW\_FIRST\_CYCLE\_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

#### 7.3.10.4.5 Open loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8316A begins to accelerate the motor in open loop. During open loop, the speed is increased with a fixed current limit. In open loop, the control PI loops for  $I_q$  and  $I_d$  actively control the currents. The angle during open loop is provided from the ramp generator as shown in 图 7-26

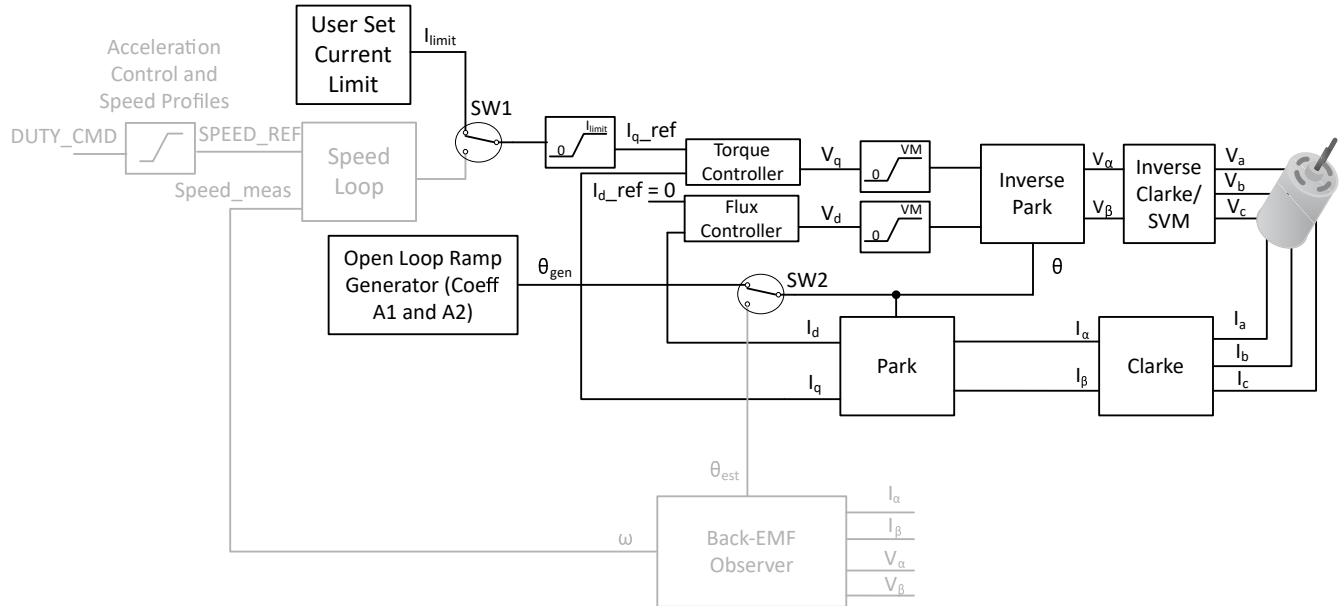


图 7-26. Open Loop

In MCF8316A, the current limit threshold is configured through `OL_ILIMIT_CONFIG` and is set by `ILIMIT` or `OL_ILIMIT` based on configuration of `OL_ILIMIT_CONFIG`. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by 方程式 5. In MCF8316A, open loop acceleration coefficients, A1 and A2 are configured through `OL_ACC_A1` and `OL_ACC_A2` respectively.

$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (5)$$

#### 7.3.10.4.6 Transition from Open to Closed Loop

Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8316A transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring `OPN_CL_HANDOFF_THR` and setting `AUTO_HANDOFF_EN` to 0b. In order to have smooth transition and avoid speed transients, the  $\theta_{\text{error}}$  ( $\theta_{\text{gen}} - \theta_{\text{est}}$ ) is decreased linearly after transition. The ramp rate of  $\theta_{\text{error}}$  reduction can be configured using `THETA_ERROR_RAMP_RATE`. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than `SPEED_REF` after transition into closed loop. In order to avoid such speed variations, configure the `IQ_RAMP_EN` to 1b, so that  $i_{q\_ref}$  decreases prior to transition into closed loop. However if the final speed reference (`SPEED_REF`) is more than two times the open loop to closed loop hand off speed (`OPN_CL_HANDOFF_THR`), then  $i_{q\_ref}$  is not decreased independent of the `IQ_RAMP_EN` setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some  $\theta_{\text{error}}$ , as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the  $\theta_{\text{error}}$  reduces to zero. The slow acceleration can be configured using `CL_SLOW_ACC`.

图 7-27 shows the control sequence in open to closed loop transition. The current  $i_{q\_ref}$  reduces to a lower value in current decay region, if `IQ_RAMP_EN` is set to 1b. If `IQ_RAMP_EN` is set to 0b, then the current decay region will not be present in the transition sequence.



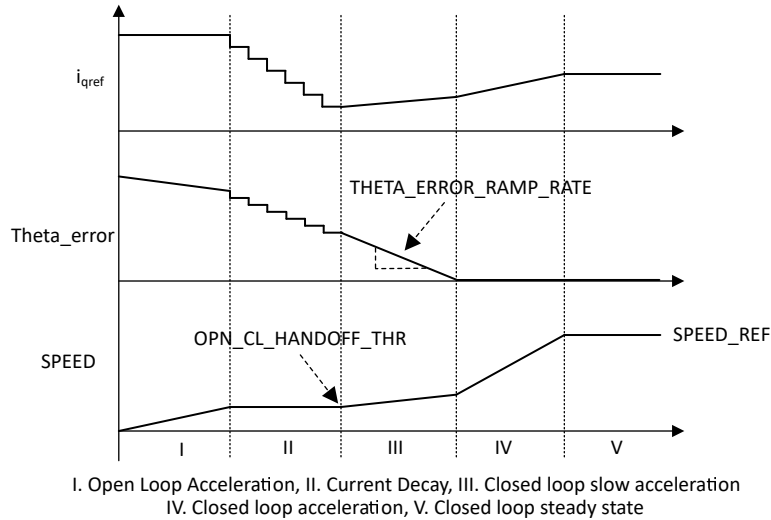


图 7-27. Control Sequence in Open to Closed Loop Transition

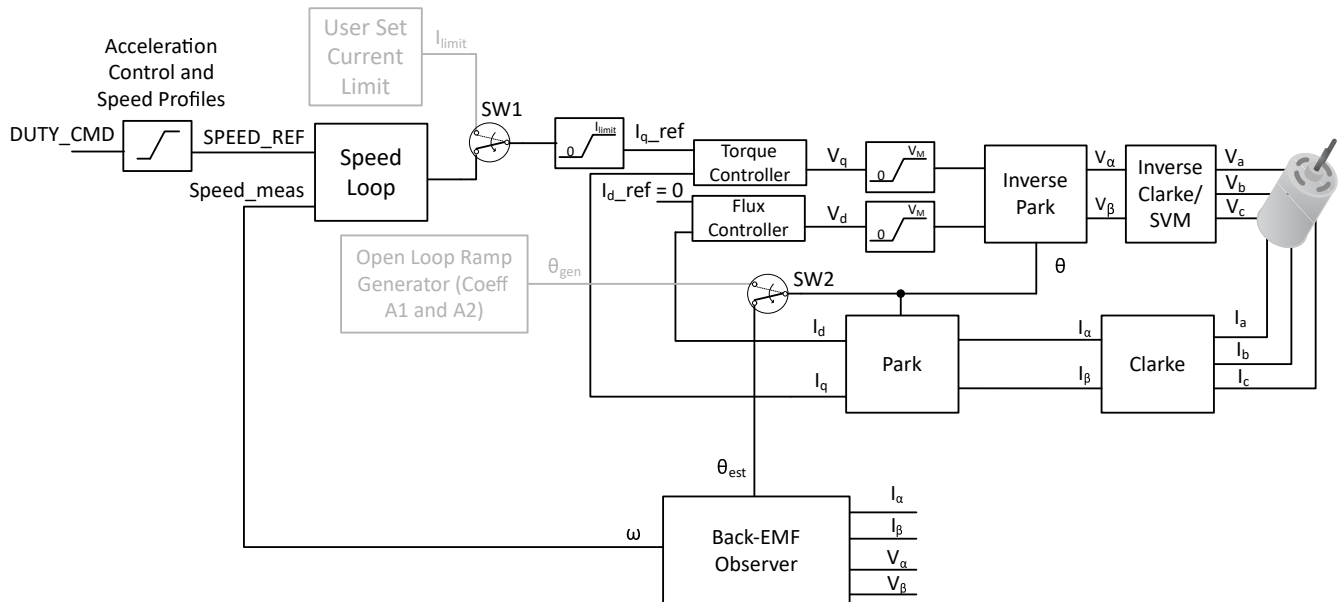


图 7-28. Open to Closed Loop Transition Control Block Diagram

### 7.3.11 Closed Loop Operation

The MCF8316A drives the motor using Field Oriented Control (FOC) as shown in 图 7-29. In closed loop operation, the motor angle ( $\Theta_{est}$ ) and speed (Speed\_meas) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero ( $i_{d\_ref} = 0$ ), which will ensure that stator and rotor field are orthogonal ( $90^\circ$  out of phase) to each other.

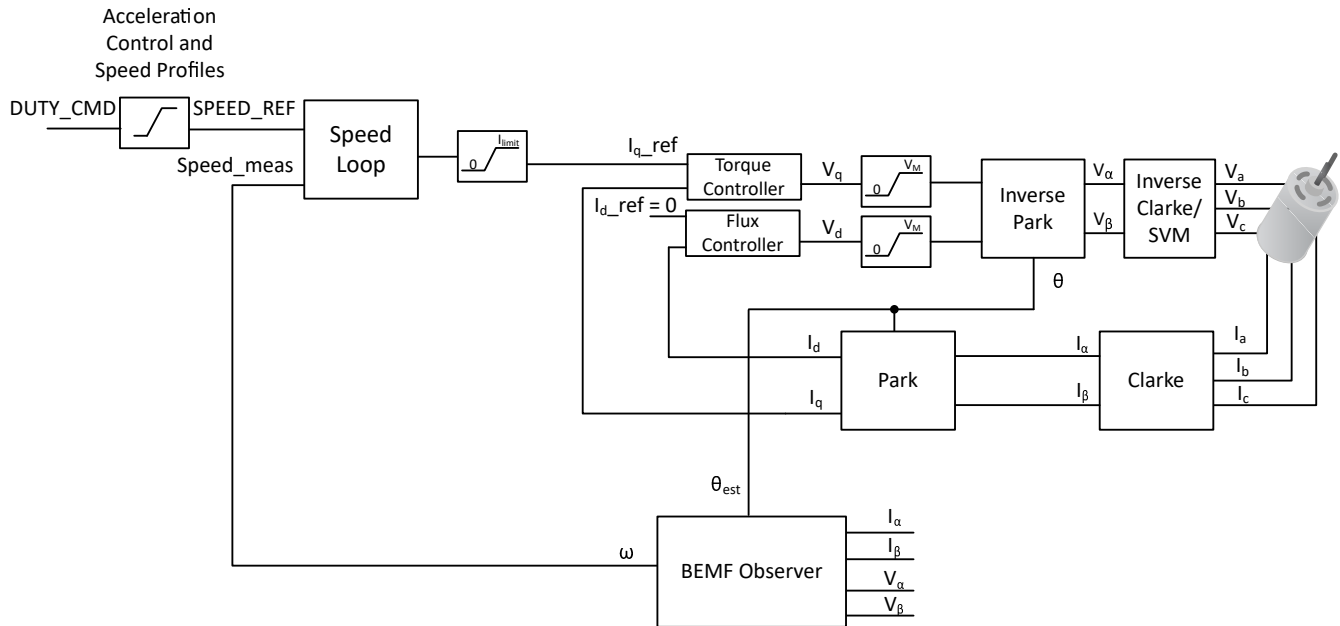


图 7-29. Closed Loop FOC Control

### 7.3.11.1 Closed loop accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the MCF8316A device provides the option of limiting the maximum rate at which the speed command can change. The closed loop acceleration rate parameter sets the maximum rate at which the speed command changes (shown in 图 7-30). In the MCF8316A, closed loop acceleration rate is configured through CL\_ACC.

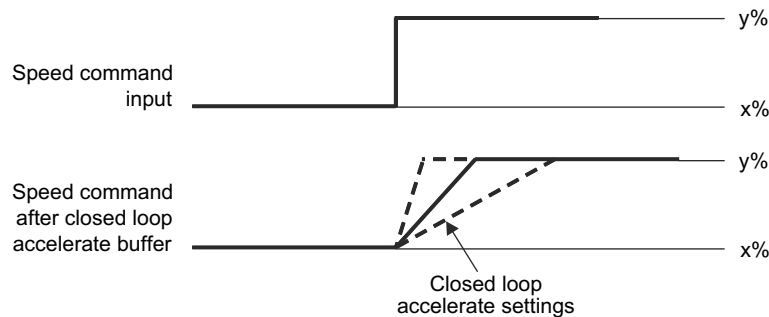


图 7-30. Closed loop accelerate

### 7.3.11.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The  $K_p$  and  $K_i$  coefficients are configured through SPD\_LOOP\_KP and SPD\_LOOP\_KI. The output of the speed loop is used to generate the current reference for torque control ( $I_{q\_ref}$ ). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED\_REF is derived from the duty command input and speed profiles configured by the user and SPEED\_MEAS is the estimated speed from the back-EMF observer.

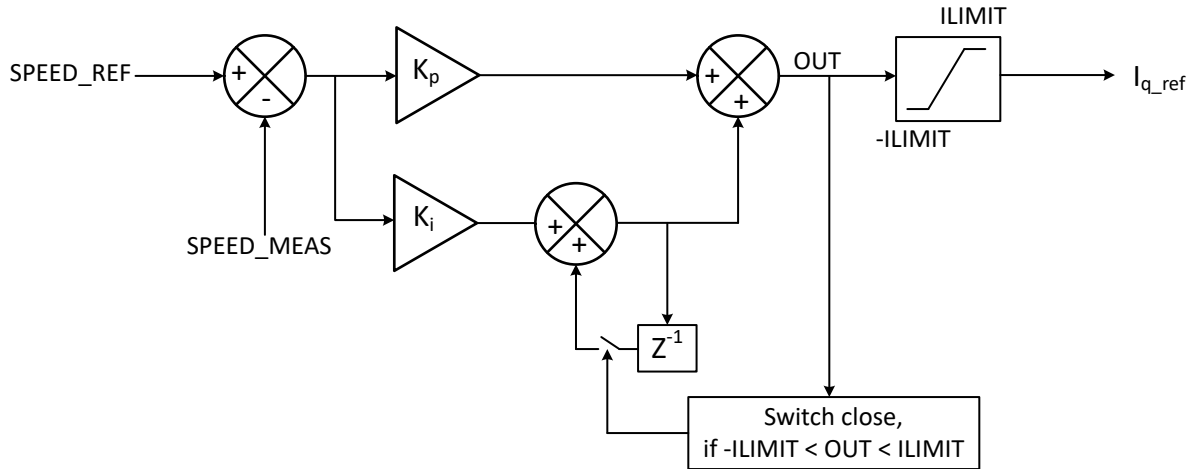


图 7-31. Speed PI Control

### 7.3.11.3 Current PI Control

The MCF8316A has two PI controllers, one each for  $I_d$  and  $I_q$  to control flux and torque separately.  $K_p$  and  $K_i$  coefficients are the same for both PI controllers and are configured through CURR\_LOOP\_KP and CURR\_LOOP\_KI. The outputs of the current control loops are used to generate voltage signals  $V_d$  and  $V_q$  to be applied to the motor. The outputs of the current loops are clamped to supply voltage  $V_M$ .  $I_d$  current PI loop is executed first and output of  $I_d$  current PI loop  $V_d$  is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.

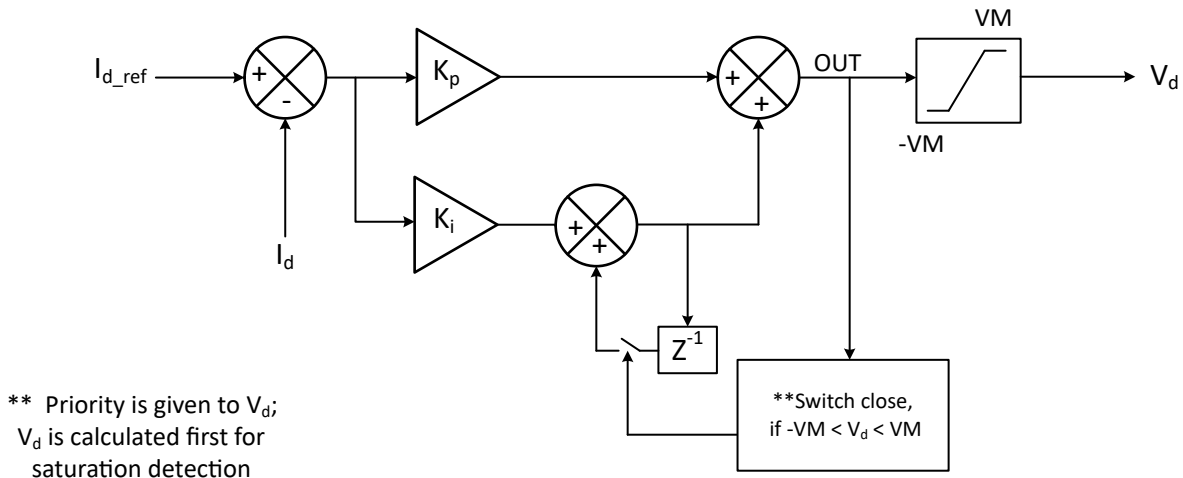


图 7-32.  $I_d$  Current PI Control

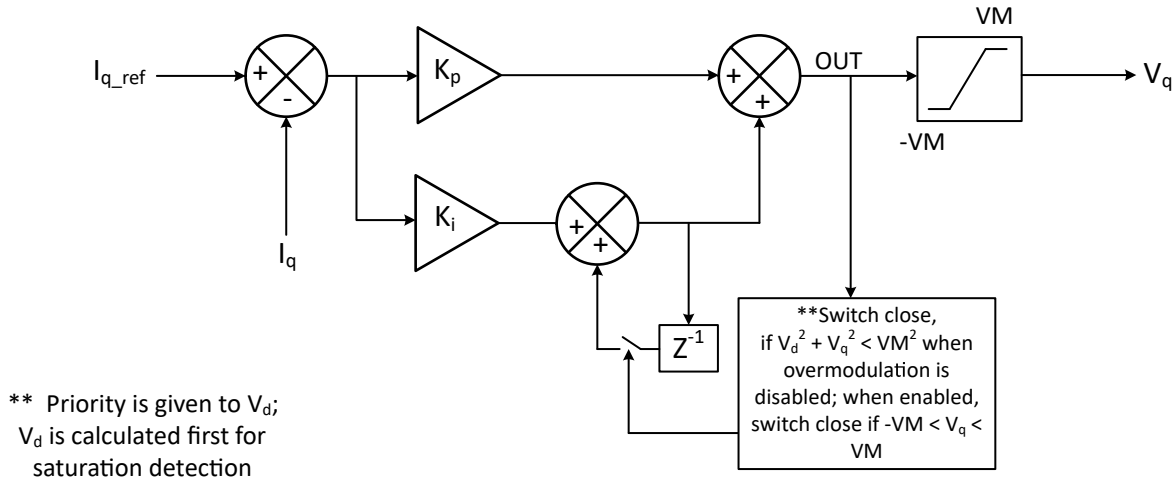


图 7-33.  $I_q$  Current PI Control

#### 7.3.11.4 Overmodulation

MCF8316A provides an overmodulation option to operate the motor at a higher speed at the same VM voltage by increasing the applied fundamental phase voltage by suitably modifying the applied PWM pattern - the higher fundamental phase voltage is accompanied by an increase in higher order harmonics. This feature can be enabled by setting OVERMODULATION\_ENABLE to 1b.

#### 7.3.12 Motor Parameters

The MCF8316A uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8316A has the capability of measuring these motor parameters in the offline state (see [Motor Parameter Extraction Tool \(MPET\)](#)). Offline measurement of parameters, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of offline motor parameter measurement is useful to account for motor to motor variation during manufacturing.

##### 7.3.12.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap,  $R_{PH}$  (denoted as  $R_{PH}$  in [图 7-34](#)). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in [图 7-34](#).

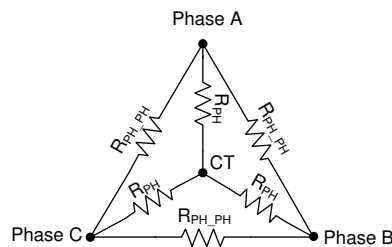


图 7-34. Motor Resistance

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent  $R_{PH}$  is to measure the resistance between two phase terminals ( $R_{PH\_PH}$ ), and then divide this value by two,  $R_{PH} = \frac{1}{2} R_{PH\_PH}$ . In wye-connected motor, if user has access to center tap (CT),  $R_{PH}$  can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance ( $R_{PH}$ ) to a nearest value from [表 7-2](#).

**表 7-2. Motor Resistance Look-Up Table**

| MOTOR_RES (HEX) | R <sub>PH</sub> (Ω)  | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) |
|-----------------|--|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|
| 0x00            | Self Measurement (see <a href="#">Motor Parameter Extraction Tool (MPET)</a> ) | 0x40            | 0.145               | 0x80            | 0.465               | 0xC0            | 2.1                 |
| 0x01            | 0.006  | 0x41            | 0.150               | 0x81            | 0.470               | 0xC1            | 2.2                 |
| 0x02            | 0.007  | 0x42            | 0.155               | 0x82            | 0.475               | 0xC2            | 2.3                 |
| 0x03            | 0.008  | 0x43            | 0.160               | 0x83            | 0.480               | 0xC3            | 2.4                 |
| 0x04            | 0.009  | 0x44            | 0.165               | 0x84            | 0.485               | 0xC4            | 2.5                 |
| 0x05            | 0.010  | 0x45            | 0.170               | 0x85            | 0.490               | 0xC5            | 2.6                 |
| 0x06            | 0.011  | 0x46            | 0.175               | 0x86            | 0.495               | 0xC6            | 2.7                 |
| 0x07            | 0.012  | 0x47            | 0.180               | 0x87            | 0.50                | 0xC7            | 2.8                 |
| 0x08            | 0.013  | 0x48            | 0.185               | 0x88            | 0.51                | 0xC8            | 2.9                 |
| 0x09            | 0.014  | 0x49            | 0.190               | 0x89            | 0.52                | 0xC9            | 3.0                 |
| 0x0A            | 0.015  | 0x4A            | 0.195               | 0x8A            | 0.53                | 0xCA            | 3.2                 |
| 0x0B            | 0.016  | 0x4B            | 0.200               | 0x8B            | 0.54                | 0xCB            | 3.4                 |
| 0x0C            | 0.017  | 0x4C            | 0.205               | 0x8C            | 0.55                | 0xCC            | 3.6                 |
| 0x0D            | 0.018  | 0x4D            | 0.210               | 0x8D            | 0.56                | 0xCD            | 3.8                 |
| 0x0E            | 0.019  | 0x4E            | 0.215               | 0x8E            | 0.57                | 0xCE            | 4.0                 |
| 0x0F            | 0.020  | 0x4F            | 0.220               | 0x8F            | 0.58                | 0xCF            | 4.2                 |
| 0x10            | 0.022  | 0x50            | 0.225               | 0x90            | 0.59                | 0xD0            | 4.4                 |
| 0x11            | 0.024  | 0x51            | 0.230               | 0x91            | 0.60                | 0xD1            | 4.6                 |
| 0x12            | 0.026  | 0x52            | 0.235               | 0x92            | 0.61                | 0xD2            | 4.8                 |
| 0x13            | 0.028  | 0x53            | 0.240               | 0x93            | 0.62                | 0xD3            | 5.0                 |
| 0x14            | 0.030  | 0x54            | 0.245               | 0x94            | 0.63                | 0xD4            | 5.2                 |
| 0x15            | 0.032  | 0x55            | 0.250               | 0x95            | 0.64                | 0xD5            | 5.4                 |
| 0x16            | 0.034  | 0x56            | 0.255               | 0x96            | 0.65                | 0xD6            | 5.6                 |
| 0x17            | 0.036  | 0x57            | 0.260               | 0x97            | 0.66                | 0xD7            | 5.8                 |
| 0x18            | 0.038  | 0x58            | 0.265               | 0x98            | 0.67                | 0xD8            | 6.0                 |
| 0x19            | 0.040  | 0x59            | 0.270               | 0x99            | 0.68                | 0xD9            | 6.2                 |
| 0x1A            | 0.042  | 0x5A            | 0.275               | 0x9A            | 0.69                | 0xDA            | 6.4                 |
| 0x1B            | 0.044  | 0x5B            | 0.280               | 0x9B            | 0.70                | 0xDB            | 6.6                 |
| 0x1C            | 0.046  | 0x5C            | 0.285               | 0x9C            | 0.72                | 0xDC            | 6.8                 |
| 0x1D            | 0.048  | 0x5D            | 0.290               | 0x9D            | 0.74                | 0xDD            | 7.0                 |
| 0x1E            | 0.050  | 0x5E            | 0.295               | 0x9E            | 0.76                | 0xDE            | 7.2                 |
| 0x1F            | 0.052  | 0x5F            | 0.300               | 0x9F            | 0.78                | 0xDF            | 7.4                 |
| 0x20            | 0.054  | 0x60            | 0.305               | 0xA0            | 0.80                | 0xE0            | 7.6                 |
| 0x21            | 0.056  | 0x61            | 0.310               | 0xA1            | 0.82                | 0xE1            | 7.8                 |
| 0x22            | 0.058  | 0x62            | 0.315               | 0xA2            | 0.84                | 0xE2            | 8.0                 |
| 0x23            | 0.060  | 0x63            | 0.320               | 0xA3            | 0.86                | 0xE3            | 8.2                 |
| 0x24            | 0.062  | 0x64            | 0.325               | 0xA4            | 0.88                | 0xE4            | 8.4                 |
| 0x25            | 0.064  | 0x65            | 0.330               | 0xA5            | 0.90                | 0xE5            | 8.6                 |
| 0x26            | 0.066  | 0x66            | 0.335               | 0xA6            | 0.92                | 0xE6            | 8.8                 |
| 0x27            | 0.068  | 0x67            | 0.340               | 0xA7            | 0.94                | 0xE7            | 9                   |
| 0x28            | 0.070  | 0x68            | 0.345               | 0xA8            | 0.96                | 0xE8            | 9.2                 |

表 7-2. Motor Resistance Look-Up Table (continued)

| MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) |
|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|
| 0x29            | 0.072               | 0x69            | 0.350               | 0xA9            | 0.98                | 0xE9            | 9.4                 |
| 0x2A            | 0.074               | 0x6A            | 0.355               | 0xAA            | 1.00                | 0xEA            | 9.6                 |
| 0x2B            | 0.076               | 0x6B            | 0.360               | 0xAB            | 1.05                | 0xEB            | 9.8                 |
| 0x2C            | 0.078               | 0x6C            | 0.365               | 0xAC            | 1.10                | 0xEC            | 10.0                |
| 0x2D            | 0.080               | 0x6D            | 0.370               | 0xAD            | 1.15                | 0xED            | 10.5                |
| 0x2E            | 0.082               | 0x6E            | 0.375               | 0xAE            | 1.20                | 0xEE            | 11.0                |
| 0x2F            | 0.084               | 0x6F            | 0.380               | 0xAF            | 1.25                | 0xEF            | 11.5                |
| 0x30            | 0.086               | 0x70            | 0.385               | 0xB0            | 1.30                | 0xF0            | 12.0                |
| 0x31            | 0.088               | 0x71            | 0.390               | 0xB1            | 1.35                | 0xF1            | 12.5                |
| 0x32            | 0.090               | 0x72            | 0.395               | 0xB2            | 1.40                | 0xF2            | 13.0                |
| 0x33            | 0.092               | 0x73            | 0.400               | 0xB3            | 1.45                | 0xF3            | 13.5                |
| 0x34            | 0.094               | 0x74            | 0.405               | 0xB4            | 1.50                | 0xF4            | 14.0                |
| 0x35            | 0.096               | 0x75            | 0.410               | 0xB5            | 1.55                | 0xF5            | 14.5                |
| 0x36            | 0.098               | 0x76            | 0.415               | 0xB6            | 1.60                | 0xF6            | 15.0                |
| 0x37            | 0.100               | 0x77            | 0.420               | 0xB7            | 1.65                | 0xF7            | 15.5                |
| 0x38            | 0.105               | 0x78            | 0.425               | 0xB8            | 1.70                | 0xF8            | 16.0                |
| 0x39            | 0.110               | 0x79            | 0.430               | 0xB9            | 1.75                | 0xF9            | 16.5                |
| 0x3A            | 0.115               | 0x7A            | 0.435               | 0xBA            | 1.80                | 0xFA            | 17.0                |
| 0x3B            | 0.120               | 0x7B            | 0.440               | 0xBB            | 1.85                | 0xFB            | 17.5                |
| 0x3C            | 0.125               | 0x7C            | 0.445               | 0xBC            | 1.90                | 0xFC            | 18.0                |
| 0x3D            | 0.130               | 0x7D            | 0.450               | 0xBD            | 1.95                | 0xFD            | 18.5                |
| 0x3E            | 0.135               | 0x7E            | 0.455               | 0xBE            | 2.00                | 0xFE            | 19.0                |
| 0x3F            | 0.140               | 0x7F            | 0.460               | 0xBF            | 2.05                | 0xFF            | 20.0                |

### 7.3.12.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap,  $L_{PH}$  (denoted as  $L_{PH}$  in 图 7-35). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in 图 7-35.

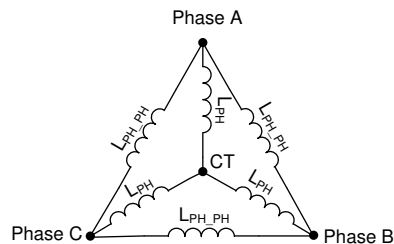


图 7-35. Motor Inductance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent  $L_{PH}$  is to measure the inductance between two phase terminals ( $L_{PH\_PH}$ ), and then divide this value by two,  $L_{PH} = \frac{1}{2} L_{PH\_PH}$ . In wye-connected motor, if user has access to center tap (CT),  $L_{PH}$  can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance ( $L_{PH}$ ) to a nearest value from 表 7-3.

**表 7-3. Motor Inductance Look-Up Table**

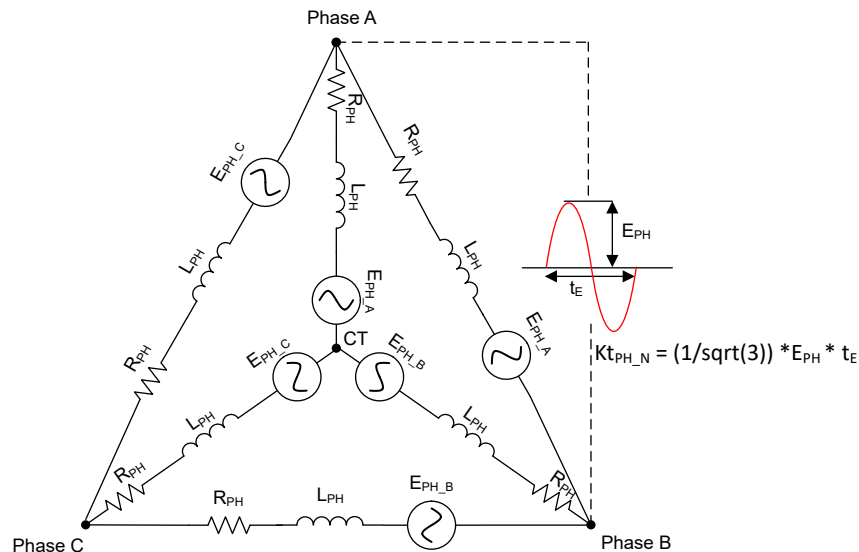
| MOTOR_IND (HEX) | L <sub>PH</sub> (mH)   | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) |
|-----------------|--|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|
| 0x00            | Self Measurement (see <a href="#">Motor Parameter Extraction Tool (MPET)</a> ) | 0x40            | 0.145                | 0x80            | 0.465                | 0xC0            | 2.1                  |
| 0x01            | 0.006  | 0x41            | 0.150                | 0x81            | 0.470                | 0xC1            | 2.2                  |
| 0x02            | 0.007  | 0x42            | 0.155                | 0x82            | 0.475                | 0xC2            | 2.3                  |
| 0x03            | 0.008  | 0x43            | 0.160                | 0x83            | 0.480                | 0xC3            | 2.4                  |
| 0x04            | 0.009  | 0x44            | 0.165                | 0x84            | 0.485                | 0xC4            | 2.5                  |
| 0x05            | 0.010  | 0x45            | 0.170                | 0x85            | 0.490                | 0xC5            | 2.6                  |
| 0x06            | 0.011  | 0x46            | 0.175                | 0x86            | 0.495                | 0xC6            | 2.7                  |
| 0x07            | 0.012  | 0x47            | 0.180                | 0x87            | 0.50                 | 0xC7            | 2.8                  |
| 0x08            | 0.013  | 0x48            | 0.185                | 0x88            | 0.51                 | 0xC8            | 2.9                  |
| 0x09            | 0.014  | 0x49            | 0.190                | 0x89            | 0.52                 | 0xC9            | 3.0                  |
| 0x0A            | 0.015  | 0x4A            | 0.195                | 0x8A            | 0.53                 | 0xCA            | 3.2                  |
| 0x0B            | 0.016  | 0x4B            | 0.200                | 0x8B            | 0.54                 | 0xCB            | 3.4                  |
| 0x0C            | 0.017  | 0x4C            | 0.205                | 0x8C            | 0.55                 | 0xCC            | 3.6                  |
| 0x0D            | 0.018  | 0x4D            | 0.210                | 0x8D            | 0.56                 | 0xCD            | 3.8                  |
| 0x0E            | 0.019  | 0x4E            | 0.215                | 0x8E            | 0.57                 | 0xCE            | 4.0                  |
| 0x0F            | 0.020  | 0x4F            | 0.220                | 0x8F            | 0.58                 | 0xCF            | 4.2                  |
| 0x10            | 0.022  | 0x50            | 0.225                | 0x90            | 0.59                 | 0xD0            | 4.4                  |
| 0x11            | 0.024  | 0x51            | 0.230                | 0x91            | 0.60                 | 0xD1            | 4.6                  |
| 0x12            | 0.026  | 0x52            | 0.235                | 0x92            | 0.61                 | 0xD2            | 4.8                  |
| 0x13            | 0.028  | 0x53            | 0.240                | 0x93            | 0.62                 | 0xD3            | 5.0                  |
| 0x14            | 0.030  | 0x54            | 0.245                | 0x94            | 0.63                 | 0xD4            | 5.2                  |
| 0x15            | 0.032  | 0x55            | 0.250                | 0x95            | 0.64                 | 0xD5            | 5.4                  |
| 0x16            | 0.034  | 0x56            | 0.255                | 0x96            | 0.65                 | 0xD6            | 5.6                  |
| 0x17            | 0.036  | 0x57            | 0.260                | 0x97            | 0.66                 | 0xD7            | 5.8                  |
| 0x18            | 0.038  | 0x58            | 0.265                | 0x98            | 0.67                 | 0xD8            | 6.0                  |
| 0x19            | 0.040  | 0x59            | 0.270                | 0x99            | 0.68                 | 0xD9            | 6.2                  |
| 0x1A            | 0.042  | 0x5A            | 0.275                | 0x9A            | 0.69                 | 0xDA            | 6.4                  |
| 0x1B            | 0.044  | 0x5B            | 0.280                | 0x9B            | 0.70                 | 0xDB            | 6.6                  |
| 0x1C            | 0.046  | 0x5C            | 0.285                | 0x9C            | 0.72                 | 0xDC            | 6.8                  |
| 0x1D            | 0.048  | 0x5D            | 0.290                | 0x9D            | 0.74                 | 0xDD            | 7.0                  |
| 0x1E            | 0.050  | 0x5E            | 0.295                | 0x9E            | 0.76                 | 0xDE            | 7.2                  |
| 0x1F            | 0.052  | 0x5F            | 0.300                | 0x9F            | 0.78                 | 0xDF            | 7.4                  |
| 0x20            | 0.054  | 0x60            | 0.305                | 0xA0            | 0.80                 | 0xE0            | 7.6                  |
| 0x21            | 0.056  | 0x61            | 0.310                | 0xA1            | 0.82                 | 0xE1            | 7.8                  |
| 0x22            | 0.058  | 0x62            | 0.315                | 0xA2            | 0.84                 | 0xE2            | 8.0                  |
| 0x23            | 0.060  | 0x63            | 0.320                | 0xA3            | 0.86                 | 0xE3            | 8.2                  |
| 0x24            | 0.062  | 0x64            | 0.325                | 0xA4            | 0.88                 | 0xE4            | 8.4                  |
| 0x25            | 0.064  | 0x65            | 0.330                | 0xA5            | 0.90                 | 0xE5            | 8.6                  |
| 0x26            | 0.066  | 0x66            | 0.335                | 0xA6            | 0.92                 | 0xE6            | 8.8                  |
| 0x27            | 0.068  | 0x67            | 0.340                | 0xA7            | 0.94                 | 0xE7            | 9                    |
| 0x28            | 0.070  | 0x68            | 0.345                | 0xA8            | 0.96                 | 0xE8            | 9.2                  |

**表 7-3. Motor Inductance Look-Up Table (continued)**

| MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) |
|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|
| 0x29            | 0.072                | 0x69            | 0.350                | 0xA9            | 0.98                 | 0xE9            | 9.4                  |
| 0x2A            | 0.074                | 0x6A            | 0.355                | 0xAA            | 1.00                 | 0xEA            | 9.6                  |
| 0x2B            | 0.076                | 0x6B            | 0.360                | 0xAB            | 1.05                 | 0xEB            | 9.8                  |
| 0x2C            | 0.078                | 0x6C            | 0.365                | 0xAC            | 1.10                 | 0xEC            | 10.0                 |
| 0x2D            | 0.080                | 0x6D            | 0.370                | 0xAD            | 1.15                 | 0xED            | 10.5                 |
| 0x2E            | 0.082                | 0x6E            | 0.375                | 0xAE            | 1.20                 | 0xEE            | 11.0                 |
| 0x2F            | 0.084                | 0x6F            | 0.380                | 0xAF            | 1.25                 | 0xEF            | 11.5                 |
| 0x30            | 0.086                | 0x70            | 0.385                | 0xB0            | 1.30                 | 0xF0            | 12.0                 |
| 0x31            | 0.088                | 0x71            | 0.390                | 0xB1            | 1.35                 | 0xF1            | 12.5                 |
| 0x32            | 0.090                | 0x72            | 0.395                | 0xB2            | 1.40                 | 0xF2            | 13.0                 |
| 0x33            | 0.092                | 0x73            | 0.400                | 0xB3            | 1.45                 | 0xF3            | 13.5                 |
| 0x34            | 0.094                | 0x74            | 0.405                | 0xB4            | 1.50                 | 0xF4            | 14.0                 |
| 0x35            | 0.096                | 0x75            | 0.410                | 0xB5            | 1.55                 | 0xF5            | 14.5                 |
| 0x36            | 0.098                | 0x76            | 0.415                | 0xB6            | 1.60                 | 0xF6            | 15.0                 |
| 0x37            | 0.100                | 0x77            | 0.420                | 0xB7            | 1.65                 | 0xF7            | 15.5                 |
| 0x38            | 0.105                | 0x78            | 0.425                | 0xB8            | 1.70                 | 0xF8            | 16.0                 |
| 0x39            | 0.110                | 0x79            | 0.430                | 0xB9            | 1.75                 | 0xF9            | 16.5                 |
| 0x3A            | 0.115                | 0x7A            | 0.435                | 0xBA            | 1.80                 | 0xFA            | 17.0                 |
| 0x3B            | 0.120                | 0x7B            | 0.440                | 0xBB            | 1.85                 | 0xFB            | 17.5                 |
| 0x3C            | 0.125                | 0x7C            | 0.445                | 0xBC            | 1.90                 | 0xFC            | 18.0                 |
| 0x3D            | 0.130                | 0x7D            | 0.450                | 0xBD            | 1.95                 | 0xFD            | 18.5                 |
| 0x3E            | 0.135                | 0x7E            | 0.455                | 0xBE            | 2.00                 | 0xFE            | 19.0                 |
| 0x3F            | 0.140                | 0x7F            | 0.460                | 0xBF            | 2.05                 | 0xFF            | 20.0                 |

**7.3.12.3 Motor Back-EMF constant**

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap,  $K_{tPH\_N}$  (denoted as  $K_{tPH\_N}$  in 图 7-36). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in 图 7-36.



**图 7-36. Motor back-EMF constant**



For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent  $K_{t_{PH\_N}}$  is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals ( $E_{PH}$ ), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by  $\sqrt{3}$  as shown in [方程式 6](#).

$$K_{t_{PH\_N}} = \frac{1}{\sqrt{3}} \times E_{PH} \times t_E \tag{6}$$

Configure the motor BEMF constant ( $K_{t_{PH\_N}}$ ) to a nearest value from [表 7-4](#).

**表 7-4. Motor BEMF constant Look-Up Table**

| MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz)  | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) |
|------------------------|--|------------------------|-------------------------|------------------------|-------------------------|------------------------|-------------------------|
| 0x00                   | Self Measurement (see <a href="#">Motor Parameter Extraction Tool (MPET)</a> ) | 0x40                   | 14.5                    | 0x80                   | 46.5                    | 0xC0                   | 210                     |
| 0x01                   | 0.6  | 0x41                   | 15.0                    | 0x81                   | 47.0                    | 0xC1                   | 220                     |
| 0x02                   | 0.7  | 0x42                   | 15.5                    | 0x82                   | 47.5                    | 0xC2                   | 230                     |
| 0x03                   | 0.8  | 0x43                   | 16.0                    | 0x83                   | 48.0                    | 0xC3                   | 240                     |
| 0x04                   | 0.9  | 0x44                   | 16.5                    | 0x84                   | 48.5                    | 0xC4                   | 250                     |
| 0x05                   | 1.0  | 0x45                   | 17.0                    | 0x85                   | 49.0                    | 0xC5                   | 260                     |
| 0x06                   | 1.1  | 0x46                   | 17.5                    | 0x86                   | 49.5                    | 0xC6                   | 270                     |
| 0x07                   | 1.2  | 0x47                   | 18.0                    | 0x87                   | 50.0                    | 0xC7                   | 280                     |
| 0x08                   | 1.3  | 0x48                   | 18.5                    | 0x88                   | 51                      | 0xC8                   | 290                     |
| 0x09                   | 1.4  | 0x49                   | 19.0                    | 0x89                   | 52                      | 0xC9                   | 300                     |
| 0x0A                   | 1.5  | 0x4A                   | 19.5                    | 0x8A                   | 53                      | 0xCA                   | 320                     |
| 0x0B                   | 1.6  | 0x4B                   | 20.0                    | 0x8B                   | 54                      | 0xCB                   | 340                     |
| 0x0C                   | 1.7  | 0x4C                   | 20.5                    | 0x8C                   | 55                      | 0xCC                   | 360                     |
| 0x0D                   | 1.8  | 0x4D                   | 21.0                    | 0x8D                   | 56                      | 0xCD                   | 380                     |
| 0x0E                   | 1.9  | 0x4E                   | 21.5                    | 0x8E                   | 57                      | 0xCE                   | 400                     |
| 0x0F                   | 2.0  | 0x4F                   | 22.0                    | 0x8F                   | 58                      | 0xCF                   | 420                     |
| 0x10                   | 2.2  | 0x50                   | 22.5                    | 0x90                   | 59                      | 0xD0                   | 440                     |
| 0x11                   | 2.4  | 0x51                   | 23.0                    | 0x91                   | 60                      | 0xD1                   | 460                     |
| 0x12                   | 2.6  | 0x52                   | 23.5                    | 0x92                   | 61                      | 0xD2                   | 480                     |
| 0x13                   | 2.8  | 0x53                   | 24.0                    | 0x93                   | 62                      | 0xD3                   | 500                     |
| 0x14                   | 3.0  | 0x54                   | 24.5                    | 0x94                   | 63                      | 0xD4                   | 520                     |
| 0x15                   | 3.2  | 0x55                   | 25.0                    | 0x95                   | 64                      | 0xD5                   | 540                     |
| 0x16                   | 3.4  | 0x56                   | 25.5                    | 0x96                   | 65                      | 0xD6                   | 560                     |
| 0x17                   | 3.6  | 0x57                   | 26.0                    | 0x97                   | 66                      | 0xD7                   | 580                     |
| 0x18                   | 3.8  | 0x58                   | 26.5                    | 0x98                   | 67                      | 0xD8                   | 600                     |
| 0x19                   | 4.0  | 0x59                   | 27.0                    | 0x99                   | 68                      | 0xD9                   | 620                     |
| 0x1A                   | 4.2  | 0x5A                   | 27.5                    | 0x9A                   | 69                      | 0xDA                   | 640                     |
| 0x1B                   | 4.4  | 0x5B                   | 28.0                    | 0x9B                   | 70                      | 0xDB                   | 660                     |
| 0x1C                   | 4.6  | 0x5C                   | 28.5                    | 0x9C                   | 72                      | 0xDC                   | 680                     |
| 0x1D                   | 4.8  | 0x5D                   | 29.0                    | 0x9D                   | 74                      | 0xDD                   | 700                     |
| 0x1E                   | 5.0  | 0x5E                   | 29.5                    | 0x9E                   | 76                      | 0xDE                   | 720                     |
| 0x1F                   | 5.2  | 0x5F                   | 30.0                    | 0x9F                   | 78                      | 0xDF                   | 740                     |
| 0x20                   | 5.4  | 0x60                   | 30.5                    | 0xA0                   | 80                      | 0xE0                   | 760                     |

表 7-4. Motor BEMF constant Look-Up Table (continued)

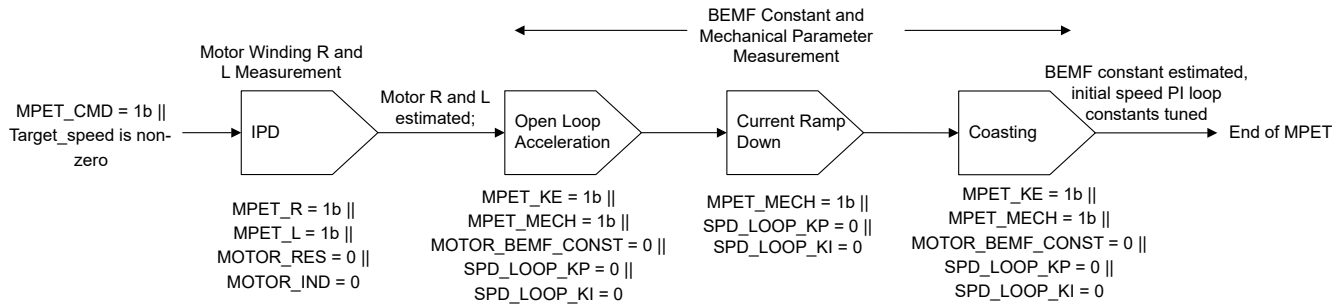
| MOTOR_BEMF_ CONST (HEX) | K <sub>tPH_N</sub> (mV/Hz) | MOTOR_BEMF_ CONST (HEX) | K <sub>tPH_N</sub> (mV/Hz) | MOTOR_BEMF_ CONST (HEX) | K <sub>tPH_N</sub> (mV/Hz) | MOTOR_BEMF_ F_CONST (HEX) | K <sub>tPH_N</sub> (mV/Hz) |
|-------------------------|----------------------------|-------------------------|----------------------------|-------------------------|----------------------------|---------------------------|----------------------------|
| 0x21                    | 5.6                        | 0x61                    | 31.0                       | 0xA1                    | 82                         | 0xE1                      | 780                        |
| 0x22                    | 5.8                        | 0x62                    | 31.5                       | 0xA2                    | 84                         | 0xE2                      | 800                        |
| 0x23                    | 6.0                        | 0x63                    | 32.0                       | 0xA3                    | 86                         | 0xE3                      | 820                        |
| 0x24                    | 6.2                        | 0x64                    | 32.5                       | 0xA4                    | 88                         | 0xE4                      | 840                        |
| 0x25                    | 6.4                        | 0x65                    | 33.0                       | 0xA5                    | 90                         | 0xE5                      | 860                        |
| 0x26                    | 6.6                        | 0x66                    | 33.5                       | 0xA6                    | 92                         | 0xE6                      | 880                        |
| 0x27                    | 6.8                        | 0x67                    | 34.0                       | 0xA7                    | 94                         | 0xE7                      | 900                        |
| 0x28                    | 7.0                        | 0x68                    | 34.5                       | 0xA8                    | 96                         | 0xE8                      | 920                        |
| 0x29                    | 7.2                        | 0x69                    | 35.0                       | 0xA9                    | 98                         | 0xE9                      | 940                        |
| 0x2A                    | 7.4                        | 0x6A                    | 35.5                       | 0xAA                    | 100                        | 0xEA                      | 960                        |
| 0x2B                    | 7.6                        | 0x6B                    | 36.0                       | 0xAB                    | 105                        | 0xEB                      | 980                        |
| 0x2C                    | 7.8                        | 0x6C                    | 36.5                       | 0xAC                    | 110                        | 0xEC                      | 1000                       |
| 0x2D                    | 8.0                        | 0x6D                    | 37.0                       | 0xAD                    | 115                        | 0xED                      | 1050                       |
| 0x2E                    | 8.2                        | 0x6E                    | 37.5                       | 0xAE                    | 120                        | 0xEE                      | 1100                       |
| 0x2F                    | 8.4                        | 0x6F                    | 38.0                       | 0xAF                    | 125                        | 0xEF                      | 1150                       |
| 0x30                    | 8.6                        | 0x70                    | 38.5                       | 0xB0                    | 130                        | 0xF0                      | 1200                       |
| 0x31                    | 8.8                        | 0x71                    | 39.0                       | 0xB1                    | 135                        | 0xF1                      | 1250                       |
| 0x32                    | 9.0                        | 0x72                    | 39.5                       | 0xB2                    | 140                        | 0xF2                      | 1300                       |
| 0x33                    | 9.2                        | 0x73                    | 40.0                       | 0xB3                    | 145                        | 0xF3                      | 1350                       |
| 0x34                    | 9.4                        | 0x74                    | 40.5                       | 0xB4                    | 150                        | 0xF4                      | 1400                       |
| 0x35                    | 9.6                        | 0x75                    | 41.0                       | 0xB5                    | 155                        | 0xF5                      | 1450                       |
| 0x36                    | 9.8                        | 0x76                    | 41.5                       | 0xB6                    | 160                        | 0xF6                      | 1500                       |
| 0x37                    | 10.0                       | 0x77                    | 42.0                       | 0xB7                    | 165                        | 0xF7                      | 1550                       |
| 0x38                    | 10.5                       | 0x78                    | 42.5                       | 0xB8                    | 170                        | 0xF8                      | 1600                       |
| 0x39                    | 11.0                       | 0x79                    | 43.0                       | 0xB9                    | 175                        | 0xF9                      | 1650                       |
| 0x3A                    | 11.5                       | 0x7A                    | 43.5                       | 0xBA                    | 180                        | 0xFA                      | 1700                       |
| 0x3B                    | 12.0                       | 0x7B                    | 44.0                       | 0xBB                    | 185                        | 0xFB                      | 1750                       |
| 0x3C                    | 12.5                       | 0x7C                    | 44.5                       | 0xBC                    | 190                        | 0xFC                      | 1800                       |
| 0x3D                    | 13.0                       | 0x7D                    | 45.0                       | 0xBD                    | 195                        | 0xFD                      | 1850                       |
| 0x3E                    | 13.5                       | 0x7E                    | 45.5                       | 0xBE                    | 200                        | 0xFE                      | 1900                       |
| 0x3F                    | 14.0                       | 0x7F                    | 46.0                       | 0xBF                    | 205                        | 0xFF                      | 2000                       |

### 7.3.13 Motor Parameter Extraction Tool (MPET)

The MCF8316A uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MCF8316A has capability of automatically measuring motor parameters in offline state, rather than having the user enter the values themselves. The MPET routine measures motor winding resistance, inductance, back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor startup to minimize the impact caused due to possible parameter variations.

图 7-37 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET\_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of four steps namely, IPD, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown below the step evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the 4 steps are completed (or

bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.



**图 7-37. MPET Sequence**

TI proprietary MPET routine includes following sequence of operation.

- IPD:** The MPET routine starts with IPD, if the user enables motor winding resistance or inductance measurement by setting MPET\_R = 1b and MPET\_L = 1b or if the user defines MOTOR\_RES = 0 or MOTOR\_IND = 0. The IPD during MPET can be configured using MPET specific configuration parameters or using the normal motor operation IPD configuration parameters. The IPD configuration selection is done using MPET\_IPD\_SELECT. With MPET\_IPD\_SELECT = 1b, the IPD current limit is configured using MPET\_IPD\_CURRENT\_LIMIT and the IPD repeat number is configured using MPET\_IPD\_FREQ. With MPET\_IPD\_SELECT = 0b, the IPD current limit and the repeat number is configured using IPD\_CURR\_THR and IPD\_REPEAT. The IPD timer over flow or the IPD current decay time more than three times the current ramp up time can result in MPET\_IPD\_FAULT. TI recommends to run the MPET multiple times to observe for consistent resistance and inductance reading.
- Open loop Acceleration:** After IPD, the MPET routine run align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET\_KE = 1b and MPET\_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET\_MECH = 0b. User can configure MPET specific open loop configuration parameters or use normal motor operation open loop configuration parameters. The open loop configuration selection is done using MPET\_KE\_MEAS\_PARAMETER\_SELECT. With MPET\_KE\_MEAS\_PARAMETER\_SELECT = 1b, the speed slew rate is defined using MPET\_OPEN\_LOOP\_SLEW\_RATE, the open loop current reference is defined using MPET\_OPEN\_LOOP\_CURR\_REF and the open loop speed reference is defined using MPET\_OPEN\_LOOP\_SPEED\_REF. With MPET\_KE\_MEAS\_PARAMETER\_SELECT = 0b, the speed slew rate is defined using OL\_ACC\_A1 and OL\_ACC\_A2, 80% of I\_LIMIT for current reference and 50% of MAX\_SPEED for speed reference.
- Current Ramp Down:** After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET\_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- Coasting:** MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT\_DETECT\_THR, the MPET\_BEMF\_FAULT is generated.

### Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR\_PARAMS Register. Setting the MPET\_WRITE\_SHADOW bit to 1, writes the MPET estimated values to the shadow registers and the user-configured (from EEPROM) values in MOTOR\_RES, MOTOR\_IND, MOTOR\_BEMF\_CONST, CURR\_LOOP\_KP, CURR\_LOOP\_KI, SPD\_LOOP\_KP and SPD\_LOOP\_KI shadow registers will be overwritten by the estimated values from MPET. If any of the shadow registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET\_WRITE\_SHADOW setting. The MPET calculates the

current loop KP and KI by using the measured resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

### 7.3.14 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the  $V_M$  voltage surges. The AVS feature works to prevent this voltage surge on  $V_M$  and can be enabled by setting AVS\_EN to 1b. AVS can be disabled by setting AVS\_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL\_DEC\_CONFIG

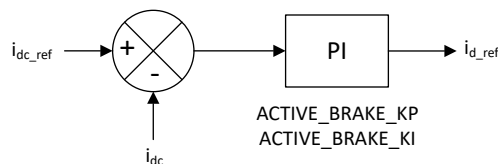
### 7.3.15 Output PWM Switching Frequency

The MCF8316A provides the option to configure the output PWM switching frequency of the MOSFETs through PWM\_FREQ\_OUT. PWM\_FREQ\_OUT has range of 10-75 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

### 7.3.16 Active Braking

Decelerating the motor quickly requires motor mechanical energy to be extracted and disposed - input DC voltage increases if this energy is returned to the DC input supply. When active braking is enabled, energy taken from DC power supply is used to brake the motor - this prevents DC voltage spike during fast deceleration. The mechanical energy of the motor and energy taken from DC source, both are dissipated within the motor itself. ACTIVE\_BRAKE\_EN should be set to 1b to enable active braking and avoid DC bus voltage spike during fast motor deceleration. Active braking can also be used during reverse drive (see [Reverse Drive](#)) or motor stop (see [Active Spin-Down](#)) to reduce the motor speed quickly without DC voltage spike.

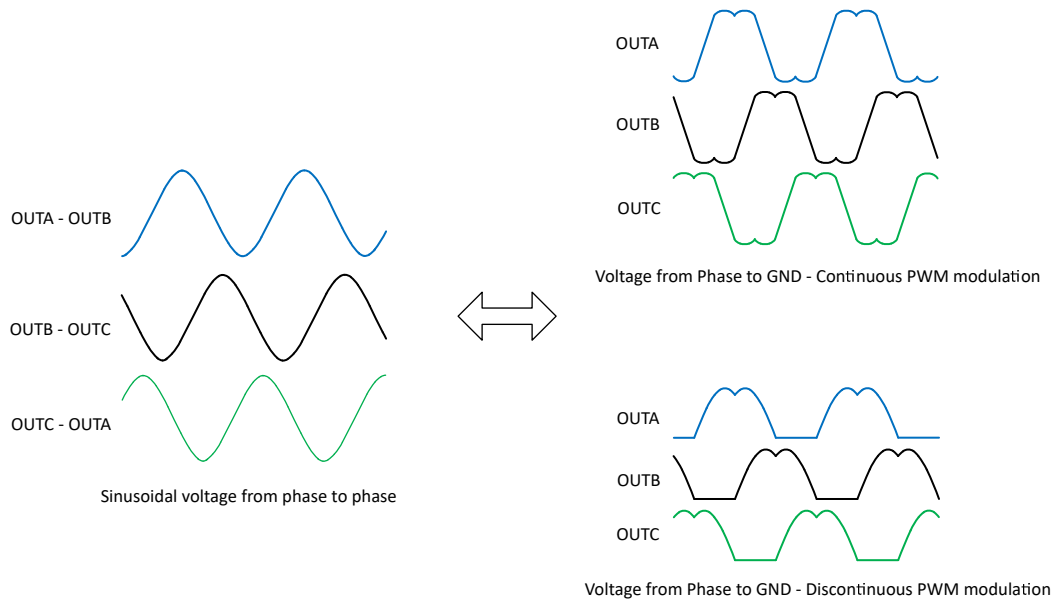
The maximum limit on the current sourced from the DC bus ( $i_{dc\_ref}$ ) during active braking can be configured using ACTIVE\_BRAKE\_CURRENT\_LIMIT. The power flow control during active braking is achieved by using both Q-axis ( $i_q$ ) and D-axis ( $i_d$ ) components of current. The D-axis current reference ( $i_{d\_ref}$ ) is generated from the error between DC bus current limit ( $i_{dc\_ref}$ ) and the estimated DC bus current ( $i_{dc}$ ) using a PI controller. The  $i_{dc}$  value is estimated from the measured phase currents, phase voltage and DC bus voltage, using power balance equation (equating the instantaneous DC bus power to sum of all three instantaneous phase power assuming 100% efficiency). During active braking, the DC bus current limit ( $i_{dc\_ref}$ ) starts from zero and linearly increases to ACTIVE\_BRAKE\_CURRENT\_LIMIT with current slew rate as defined by ACTIVE\_BRAKE\_BUS\_CURRENT\_SLEW\_RATE. The gain constants of PI controller can be configured using ACTIVE\_BRAKE\_KP and ACTIVE\_BRAKE\_KI. [图 7-38](#) shows the active braking  $i_d$  current control loop.



**图 7-38. Active Braking Current Control Loop for  $i_{d\_ref}$**

### 7.3.17 PWM Modulation Schemes

The MCF8316 supports two different modulation schemes, namely, continuous and discontinuous space vector PWM modulation schemes. In continuous PWM modulation, all the three phases switch all the time as per the defined switching frequency. In discontinuous PWM modulation, one of the phases is clamped to ground for 120° electrical period, and the other two phases are pulse width modulated. The modulation scheme is configured using PWM\_MODE. [图 7-39](#) shows the modulated average phase voltages for different modulation schemes.



**图 7-39. Continuous and Discontinuous PWM Modulation Phase Voltages**

Continuous modulation helps in reducing current ripple for motors having low inductance but it results in higher switching losses because all three phases are switching. Discontinuous modulation has lower switching losses due to only two phases switching at a time, but higher current ripple.

### 7.3.18 Dead Time Compensation

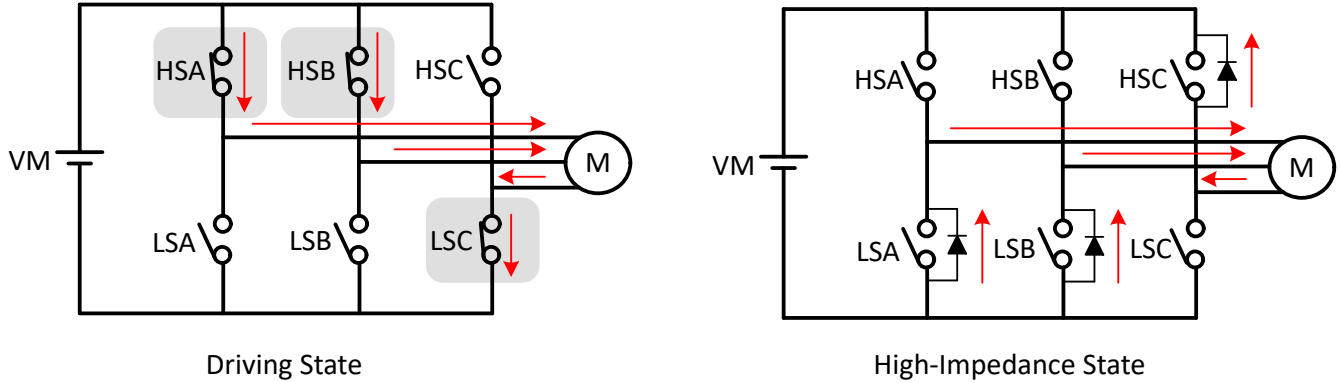
Dead time is inserted between the switching instants of high-side and low-side MOSFET in a half bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. The distortion in current waveform due to dead time appear as sixth harmonic of fundamental frequency in the dq reference frame. The MCF8316 integrates a proprietary dead time compensation using a resonant controller to control the sixth harmonic component in phase current to zero, ensuring that the current distortion due to dead time is alleviated. The resonant controller is employed in both  $i_q$  and  $i_d$  control paths. The dead time compensation can be enabled or disabled by configuring DEADTIME\_COMP\_EN.

### 7.3.19 Motor Stop Options

The MCF8316A provides different options for stopping the motor which can be configured by MTR\_STOP.

#### 7.3.19.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR\_STOP to 000b. When motor stop command is received, the MCF8316A will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCF8316A transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example [图 7-40](#)).



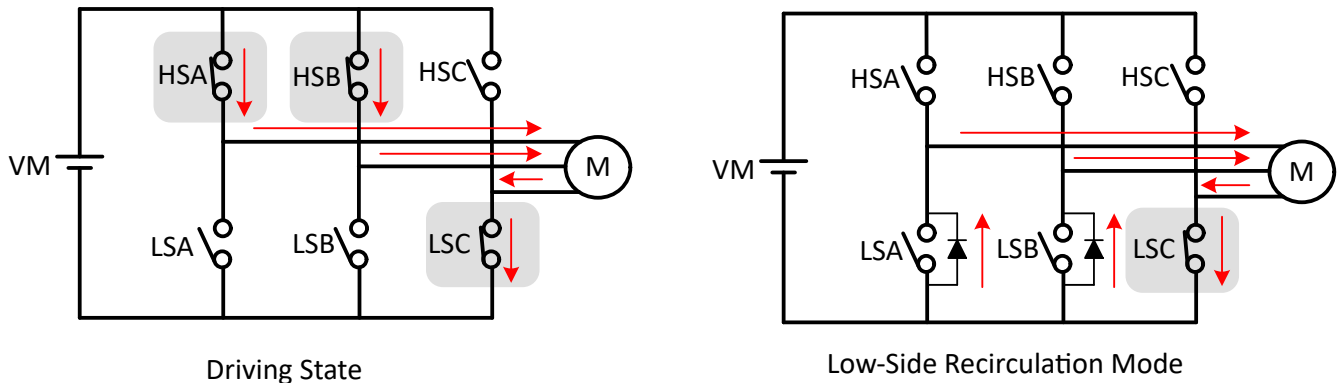
**图 7-40. Coast (Hi-Z) Mode**

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET(HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

**7.3.19.2 Recirculation Mode**

Recirculation mode is configured by setting MTR\_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCF8316A allows current to circulate within the MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

Depending on the phase voltage pattern at the time of receiving the stop command, either low-side (see [图 7-41](#)) or high-side recirculation (see [图 7-42](#)) will be used to stop the motor without sending the inductive energy back to the DC input supply.



**图 7-41. Low-Side Recirculation**

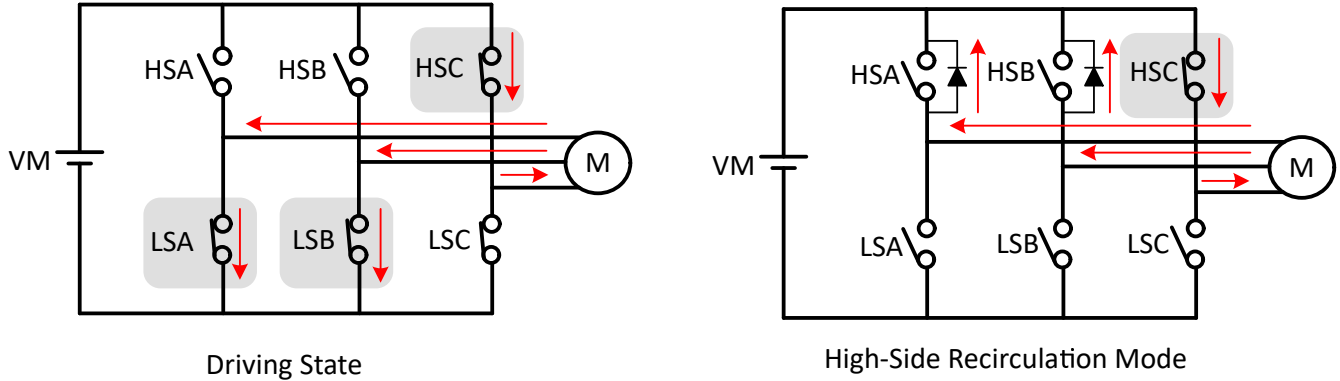


图 7-42. High-Side Recirculation

### 7.3.19.3 Low-Side Braking

Low-side braking mode is configured by setting MTR\_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON (see example 图 7-43) for a time configured by MTR\_STOP\_BRK\_TIME. If the motor speed is below BRAKE\_SPEED\_THRESHOLD prior to receiving stop command, then the MCF8316A transitions directly into the brake state. After applying the brake for MTR\_STOP\_BRK\_TIME, the MCF8316A transitions into the Hi-Z state by turning OFF all MOSFETs.

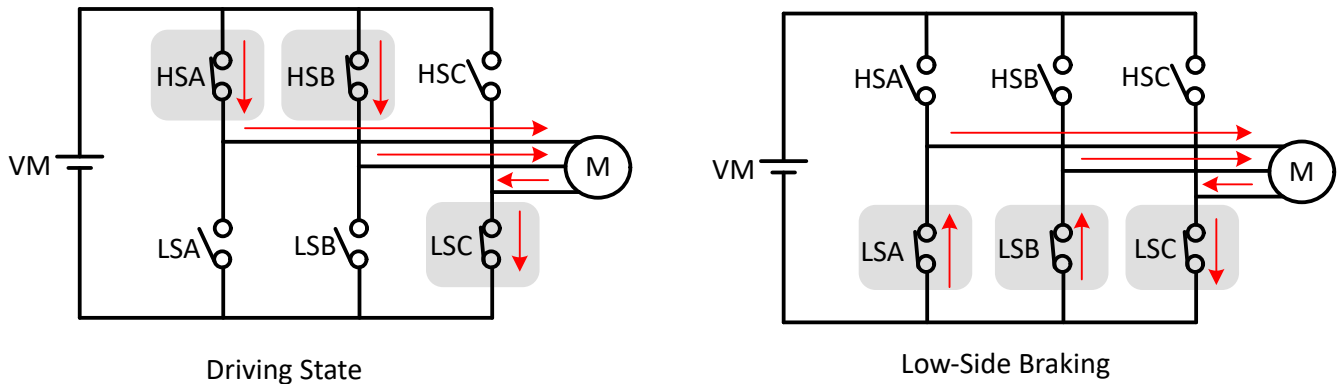


图 7-43. Low-Side Braking

The MCF8316A can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8316A stays in low-side brake state till BRAKE pin changes to LOW state.

### 7.3.19.4 High-Side Braking

High-side braking mode is configured by setting MTR\_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all high-side MOSFETs ON (see example 图 7-44) for a time configured by MTR\_STOP\_BRK\_TIME. If the motor speed is below BRAKE\_SPEED\_THRESHOLD prior to receiving stop command, then the MCF8316A transitions directly into the brake state. After applying the brake for MTR\_STOP\_BRK\_TIME, the MCF8316A transitions into Hi-Z state by turning OFF all MOSFETs.

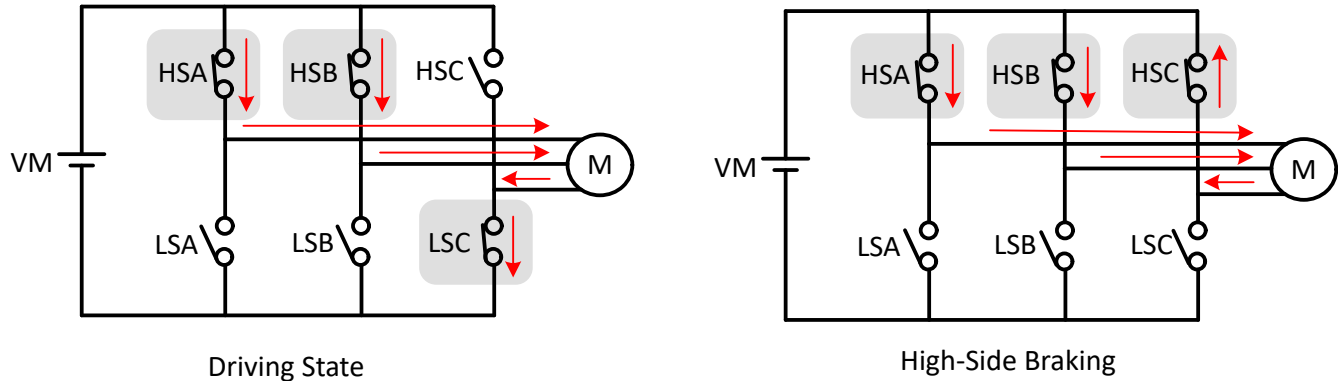


图 7-44. High-Side Braking

### 7.3.19.5 Active Spin-Down

Active spin down mode is configured by setting MTR\_STOP to 100b. When a motor stop command is received, the MCF8316A reduces SPEED\_REF to ACT\_SPIN\_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing SPEED\_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT\_SPIN\_THR needs to be configured high enough for MCF8316A to not lose synchronization with the motor.

### 7.3.19.6 Align Braking

Align braking mode is configured by setting MTR\_STOP to 101b. The MCF8316A can also enter align brake state through the BRAKE pin. In this mode, the MCF8316A aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by MTR\_STOP\_BRK\_TIME. The phase pattern during align is generated based on the angle at which align needs to be performed and this angle can be configured through ALIGN\_ANGLE or the last commutation angle. ALIGN\_BRAKE\_ANGLE\_SEL can be configured to decide which align angle is to be used by MCF8316A. The current limit threshold during align braking is configured through ALIGN\_OR\_SLOW\_CURRENT\_LIMIT.

## 7.3.20 FG Configuration

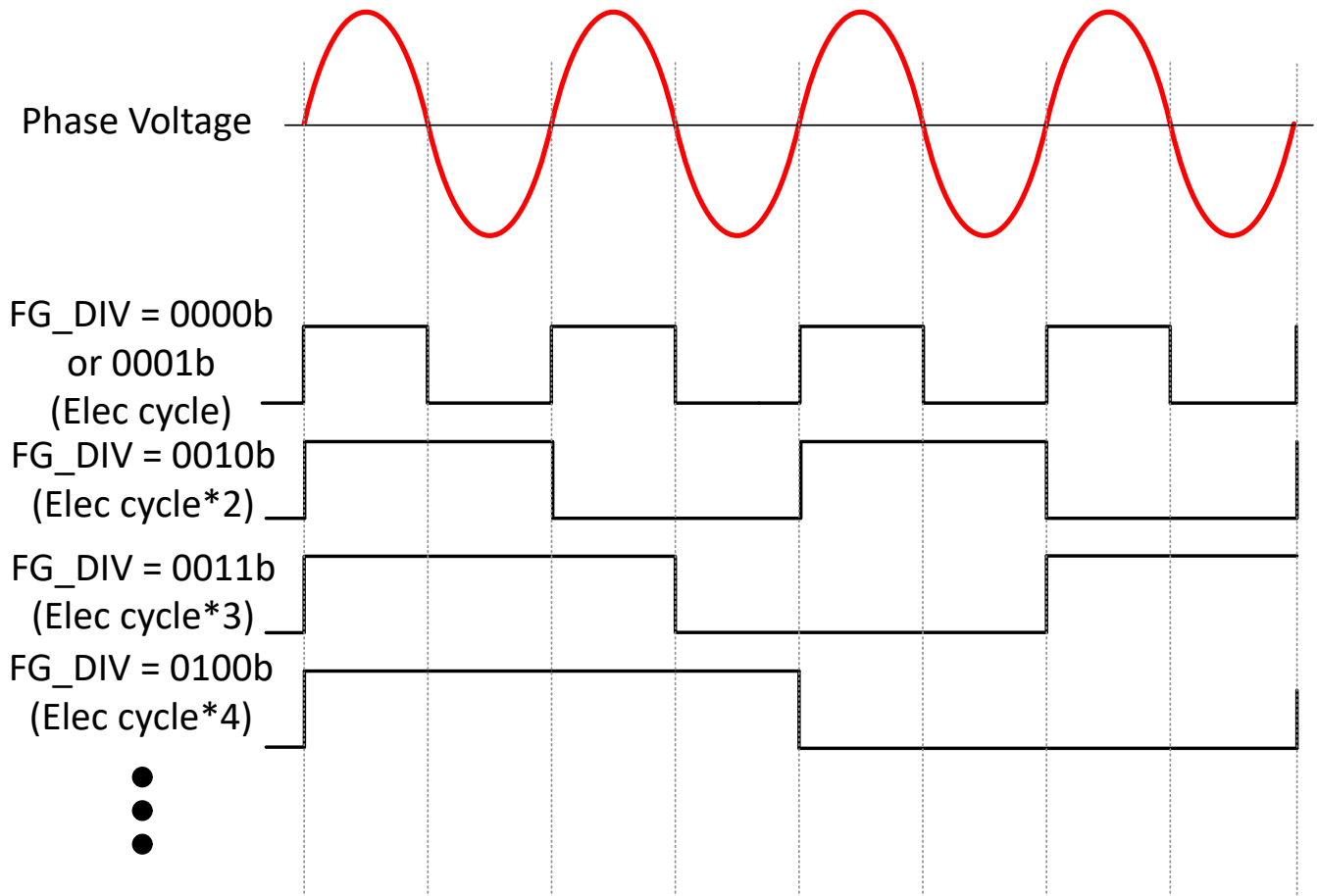
The MCF8316A provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8316A, the FG pin output is configured through FG\_CONFIG. When FG\_CONFIG is configured to 0b, the FG output is active as long as the MCF8316A is driving the motor. When FG\_CONFIG is configured to 1b, the MCF8316A provides an FG output until the motor back-EMF falls below FG\_BEMF\_THR.

### 7.3.20.1 FG Output Frequency

The FG output frequency can be configured by FG\_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG\_DIV configurations can accomplish this for 2-pole up to 30-pole motors.

图 7-45 shows the FG output when MCF8316A has been configured to provide FG pulses once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.





**图 7-45. FG Frequency Divider**

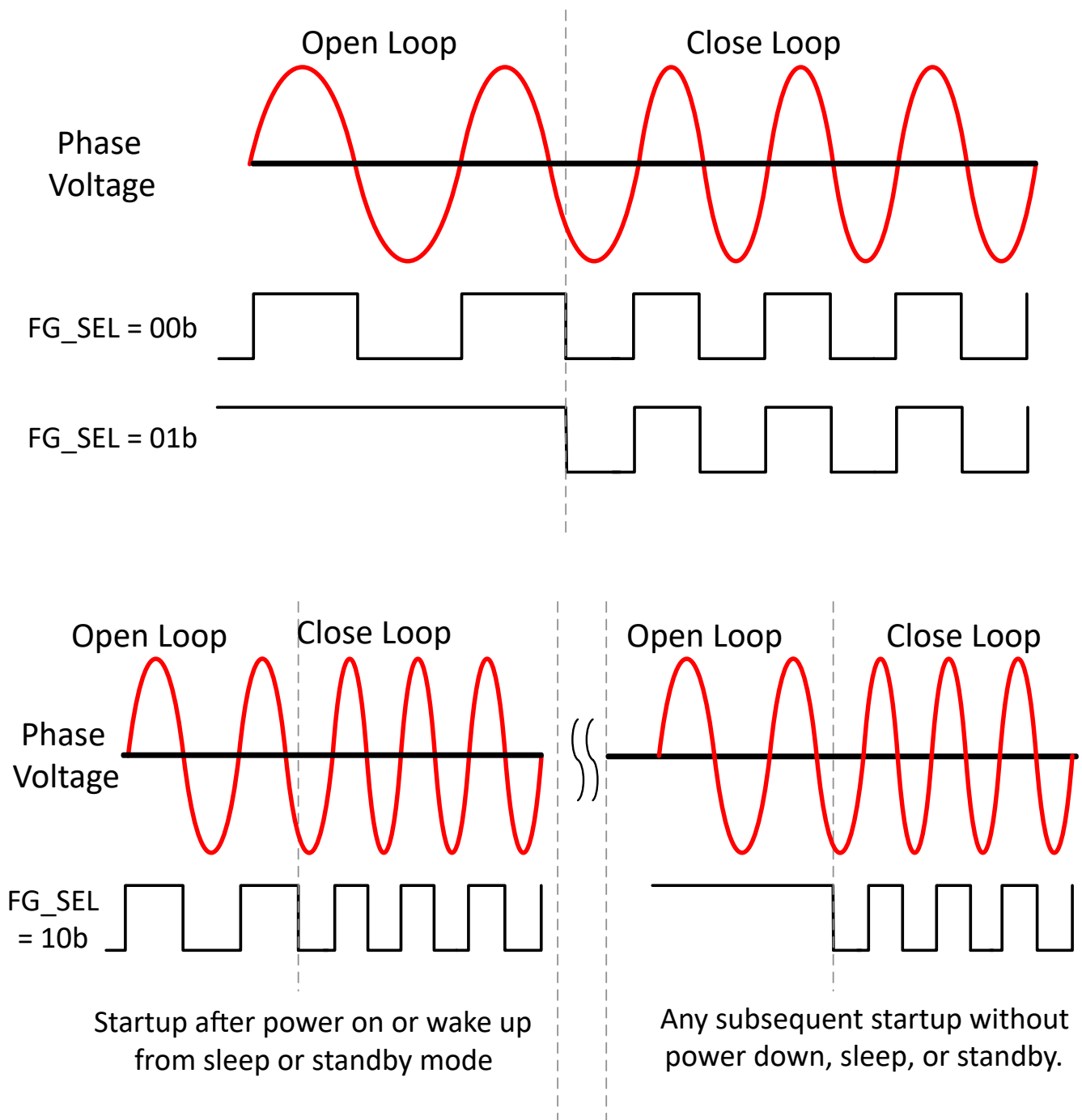
### 7.3.20.2 FG Open-Loop and Lock Behavior

During closed loop operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. During motor-lock condition, the FG output is driven high.

The MCF8316A provides three options for controlling the FG output during open loop, as shown in [图 7-46](#). The selection of these options is configured through FG\_SEL.

If FG\_SEL is set to,

- 00b: When in open loop, the FG output is based on the driving frequency.
- 01b: When in open loop, the FG output will be driven high.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be held high during open loop operation in subsequent start-up cycles.



**图 7-46. FG Behavior During Open Loop**

### 7.3.21 DC Bus Current Limit

The DC bus current limit feature can be used in applications to limit the current supplied by source without entering the constant current mode. The DC bus current limit feature can be enabled by setting `BUS_CURRENT_LIMIT_ENABLE` to 1b. The DC bus current limit threshold can be configured using `BUS_CURRENT_LIMIT`. The DC bus current limit limits the speed reference and a functional diagram is shown in [图 7-47](#). Enabling this feature may restrict the speed of the motor so that current drawn from source is limited. The algorithm estimates the bus current using the measured phase currents, phase voltage and DC bus voltage. The current limit status is reported on `BUS_CURRENT_LIMIT_STATUS`.

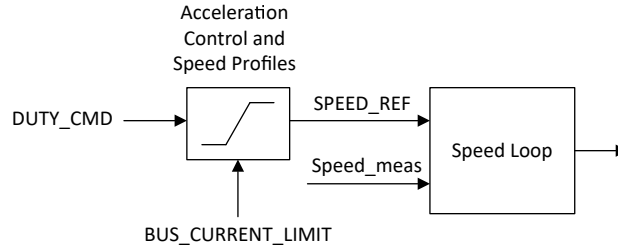


图 7-47. DC Bus Current Limit Functional Block Diagram

### 7.3.22 Protections

The MCF8316A is protected from a host of fault events including motor lock, VM undervoltage, AVDD undervoltage, buck undervoltage, charge pump undervoltage, overtemperature and overcurrent events. 表 7-5 summarizes the response, recovery modes, power stage status, reporting mechanism for different faults.

表 7-5. Fault Action and Response

| FAULT                                  | CONDITION                 | CONFIGURATION  | REPORT                                       | H-BRIDGE | LOGIC    | RECOVERY                                |
|--|---------------------------|----------------|--|----------|----------|---|
| VM undervoltage (NPOR)                 | $V_{VM} < V_{UVLO}$       | —              | —  | Hi-Z     | Disabled | Automatic:<br>$V_{VM} > V_{UVLO}$       |
| AVDD undervoltage (NPOR)               | $V_{AVDD} < V_{AVDD\_UV}$ | —              | —  | Hi-Z     | Disabled | Automatic:<br>$V_{AVDD} > V_{AVDD\_UV}$ |
| Buck undervoltage (BUCK_UV)            | $V_{FB\_BK} < V_{BK\_UV}$ | —              | —  | Hi-Z     | Disabled | Automatic:<br>$V_{FB\_BK} > V_{BK\_UV}$ |
| Charge pump undervoltage (VCP_UV)      | $V_{CP} < V_{CPUV}$       | —              | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z     | Active   | Automatic:<br>$V_{VCP} > V_{CPUV}$      |
| OverVoltage Protection (OVP)           | $V_{VM} > V_{OVP}$        | OVP_EN = 0b    | None   | Active   | Active   | No action (OVP Disabled)                |
|  |                           | OVP_EN = 1b    | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z     | Active   | Automatic:<br>$V_{VM} < V_{OVP}$        |
| Overcurrent Protection (OCP)           | $I_{PHASE} > I_{OCP}$     | OCP_MODE = 00b | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z     | Active   | Latched:<br>CLR_FLT                     |
|  |                           | OCP_MODE = 01b | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z     | Active   | Retry:<br>$t_{RETRY}$                   |
|  |                           | OCP_MODE = 10b | nFAULT and GATE_DRIVER_FAULT_STATUS register | Active   | Active   | No action                               |
|  |                           | OCP_MODE = 11b | None   | Active   | Active   | No action                               |
| Buck Overcurrent Protection (BUCK_OCP) | $I_{BK} > I_{BK\_OCP}$    | —              | —  | Hi-Z     | Disabled | Retry:<br>$t_{RETRY}$                   |

表 7-5. Fault Action and Response (continued)

| FAULT  | CONDITION  | CONFIGURATION               | REPORT                                      | H-BRIDGE        | LOGIC  | RECOVERY                      |
|--|--|-----------------------------|---|-----------------|--------|-------------------------------|
| Motor Lock<br>(MTR_LCK )                                   | Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF | MTR_LCK_MODE = 0000b        | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT              |
|  |  | MTR_LCK_MODE = 0001b        | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Latched: CLR_FLT              |
|  |  | MTR_LCK_MODE = 0010b        | nFAULT and CONTROLLER_FAULT_STATUS register | High side brake | Active | Latched: CLR_FLT              |
|  |  | MTR_LCK_MODE = 0011b        | nFAULT and CONTROLLER_FAULT_STATUS register | Low side brake  | Active | Latched: CLR_FLT              |
|  |  | MTR_LCK_MODE = 0100b        | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | MTR_LCK_MODE = 0101b        | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | MTR_LCK_MODE = 0110b        | nFAULT and CONTROLLER_FAULT_STATUS register | High side brake | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | MTR_LCK_MODE = 0111b        | nFAULT and CONTROLLER_FAULT_STATUS register | Low side brake  | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | MTR_LCK_MODE = 1000b        | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active | No action                     |
|  |  | MTR_LCK_MODE = 1xx1b        | None  | Active          | Active | No action                     |
| Hardware Lock-Detection Current Limit<br>(HW_LOCK_ILIMIT ) | V <sub>sox</sub> > HW_LOCK_ILIMIT                        | HW_LOCK_ILIMIT_MODE = 0000b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT              |
|  |  | HW_LOCK_ILIMIT_MODE = 0001b | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Latched: CLR_FLT              |
|  |  | HW_LOCK_ILIMIT_MODE = 0010b | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active | Latched: CLR_FLT              |
|  |  | HW_LOCK_ILIMIT_MODE = 0011b | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active | Latched: CLR_FLT              |
|  |  | HW_LOCK_ILIMIT_MODE = 0100b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | HW_LOCK_ILIMIT_MODE = 0101b | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | HW_LOCK_ILIMIT_MODE = 0110b | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | HW_LOCK_ILIMIT_MODE = 0111b | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active | Retry: t <sub>LCK_RETRY</sub> |
|  |  | HW_LOCK_ILIMIT_MODE = 1000b | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active | No action                     |
|  |  | HW_LOCK_ILIMIT_MODE = 1xx1b | None  | Active          | Active | No action                     |

**表 7-5. Fault Action and Response (continued)**

| FAULT   | CONDITION  | CONFIGURATION                        | REPORT                                      | H-BRIDGE        | LOGIC  | RECOVERY   |
|---|--|--------------------------------------|---|-----------------|--------|--|
| Software Lock-Detection Current Limit (LOCK_ILIMIT) | $V_{SOX} > LOCK\_ILIMIT$   | LOCK_ILIMIT_MODE = 0000b             | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT                                     |
|   |  | LOCK_ILIMIT_MODE = 0001b             | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Latched: CLR_FLT                                     |
|   |  | LOCK_ILIMIT_MODE = 0010b             | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active | Latched: CLR_FLT                                     |
|   |  | LOCK_ILIMIT_MODE = 0011b             | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active | Latched: CLR_FLT                                     |
|   |  | LOCK_ILIMIT_MODE = 0100b             | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Retry: $t_{LCK\_RETRY}$                              |
|   |  | LOCK_ILIMIT_MODE = 0101b             | nFAULT and CONTROLLER_FAULT_STATUS register | Recirculation   | Active | Retry: $t_{LCK\_RETRY}$                              |
|   |  | LOCK_ILIMIT_MODE = 0110b             | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active | Retry: $t_{LCK\_RETRY}$                              |
|   |  | LOCK_ILIMIT_MODE = 0111b             | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active | Retry: $t_{LCK\_RETRY}$                              |
|   |  | LOCK_ILIMIT_MODE = 1000b             | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active | No action  |
| LOCK_ILIMIT_MODE = 1xx1b                            | None   | Active                               | Active                                      | No action       |        |  |
| IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)   | IPD TIME > 500ms (approx), during IPD current ramp up or ramp down | IPD_TIMEOUT_FAULT_EN = 1             | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT                                     |
| IP Frequency Fault (IPD_FREQ_FAULT)                 | IPD pulse before the current decay in previous IPD                 | IPD_TIMEOUT_FAULT_EN = 1             | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT                                     |
| MPET IPD Fault (MPET_IPD_FAULT)                     | Same as IPD Timeout Fault.   | MPET_CMD = 1 or MPET_R or MPET_L = 1 | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT                                     |
| MPET Back-EMF Fault (MPET_BEMF_FAULT)               | Motor Back EMF < STAT_DETECT_THR                                   | MPET_CMD = 1 or MPET_KE = 1          | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Latched: CLR_FLT                                     |
| Thermal warning (OTW)                               | $T_J > T_{OTW}$  | OTW_REP = 0b                         | None  | Active          | Active | No action  |
|   |  | OTW_REP = 1b                         | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active | Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$<br>CLR_FLT |
| Thermal shutdown (TSD)                              | $T_J > T_{TSD}$  | —                                    | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active | Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$<br>CLR_FLT |

### 7.3.22.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the  $V_{UVLO}$  threshold (VM UVLO falling threshold), all the integrated FETs, driver charge-pump and digital logic are disabled as shown in 图 7-48. MCF8316A goes into reset state whenever VM UVLO event occurs.

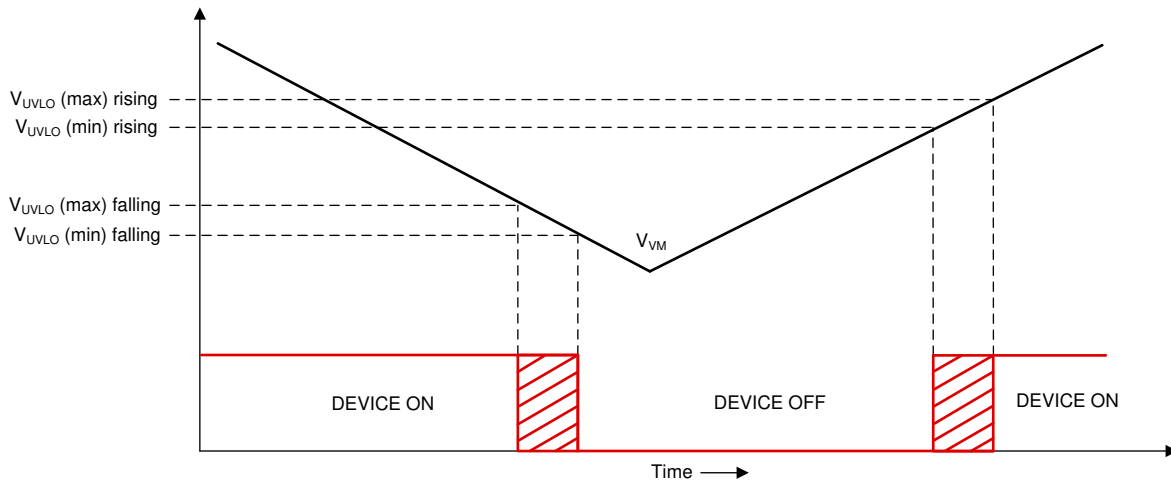


图 7-48. VM Supply Undervoltage Lockout

### 7.3.22.2 AVDD Undervoltage Lockout (AVDD\_UV)

If at any time the voltage on the AVDD pin falls lower than the  $V_{AVDD\_UV}$  threshold, all the integrated FETs, driver charge-pump and digital logic controller are disabled. Since internal circuitry in MCF8316A is powered through the AVDD regulator, MCF8316A goes into reset state whenever AVDD UV event occurs.

### 7.3.22.3 BUCK Undervoltage Lockout (BUCK\_UV)

If at any time the input supply voltage on the FB\_BK pin falls lower than the  $V_{BK\_UVLO}$  threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled. Since internal circuitry in MCF8316A is powered through the buck regulator, MCF8316A goes into reset state whenever buck UV event occurs.

### 7.3.22.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the  $V_{CPUV}$  threshold, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT and VCP\_UV bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The VCP\_UV bit stays set until cleared through the CLR\_FLT bit.

### 7.3.22.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher lower than the  $V_{OVP}$  threshold voltage, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT and OVP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR\_FLT bit. Setting the OVP\_EN to 1b enables this protection feature.

The OVP threshold can be set to 20-V or 32-V based on the OVP\_SEL bit.

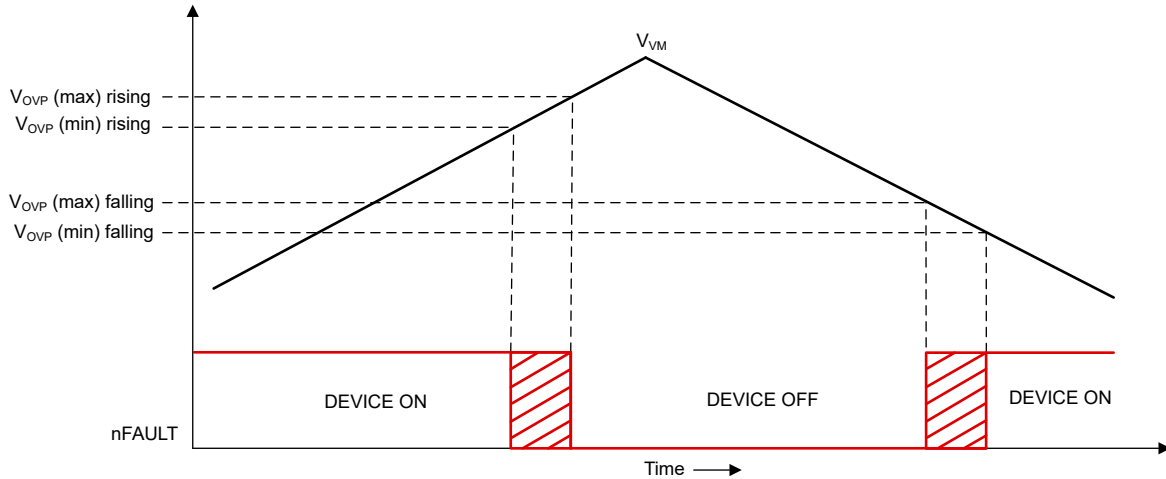


图 7-49. Over Voltage Protection

### 7.3.22.6 Overcurrent Protection (OCP)

MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the  $I_{OCP}$  threshold for longer than the  $t_{OCP}$  deglitch time, an OCP event is recognized and action is taken according to the OCP\_MODE bit. The  $I_{OCP}$  threshold is set through the OCP\_LVL, the  $t_{OCP\_DEG}$  is set through the OCP\_DEG and the OCP\_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only and OCP disabled.

#### 7.3.22.6.1 OCP Latched Shutdown (OCP\_MODE = 00b)

When an OCP event happens in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear fault command is issued through the CLR\_FLT bit.

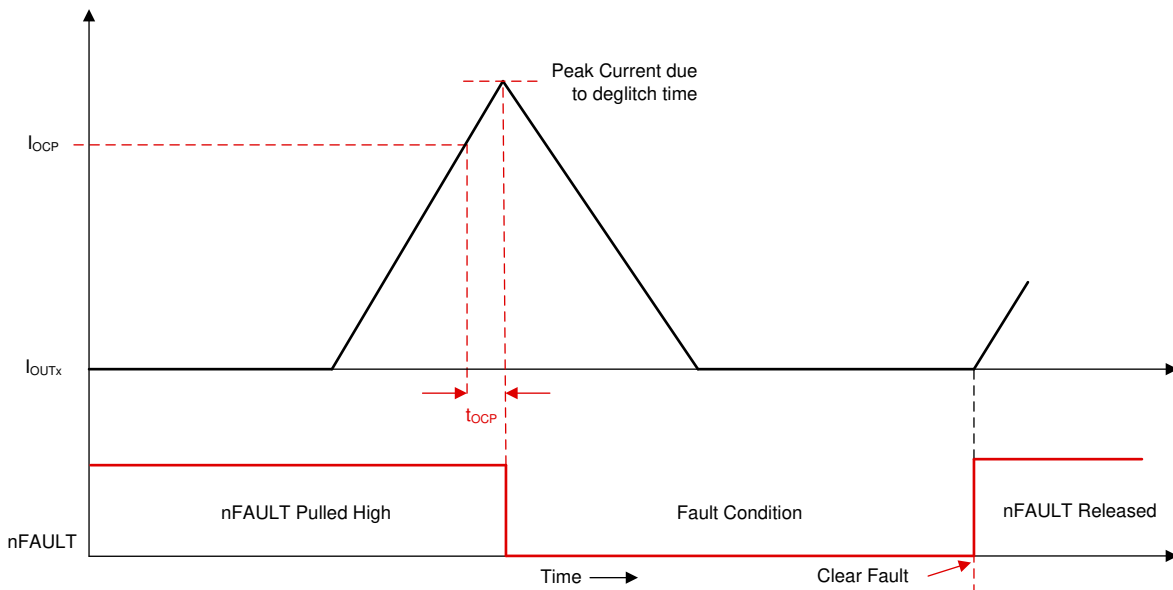


图 7-50. Overcurrent Protection - Latched Shutdown Mode

#### 7.3.22.6.2 OCP Automatic Retry (OCP\_MODE = 01b)

When an OCP event happens in this mode, all the FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the fault status registers.

Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{\text{RETRY}}$  (OCP\_RETRY) time elapses. The DRIVER\_FAULT bit is reset to 0b after the  $t_{\text{RETRY}}$  period expires. The OCP, and corresponding FET's OCP bits are set to 1b until cleared through the CLR\_FLT bit.

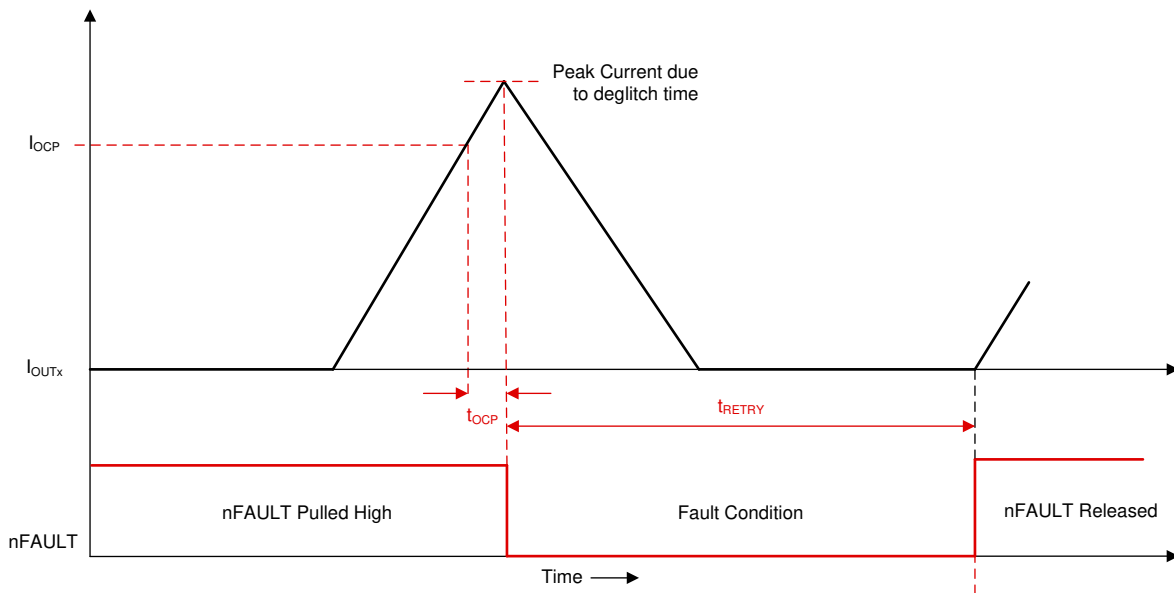


图 7-51. Overcurrent Protection - Automatic Retry Mode

#### 7.3.22.6.3 OCP Report Only (OCP\_MODE = 10b)

No protective action is taken when an OCP event happens in this mode. The overcurrent event is reported by setting the DRIVER\_FAULT, OCP, and corresponding FET's OCP bits to 1b in the fault status registers. If ALARM\_PIN\_DIS is set to 0b, nFAULT is driven low to report the fault. If ALARM\_PIN\_DIS is set to 1b, nFAULT is not driven low. The device continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears when the OCP condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.6.4 OCP Disabled (OCP\_MODE = 11b)

No action is taken when an OCP event happens in this mode.

#### 7.3.22.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the  $I_{\text{BK\_OCP}}$  threshold for a time longer than the deglitch time ( $t_{\text{OCP\_DEG}}$ ), a buck OCP event is recognized. MCF8316A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8316A is powered from the buck regulator output.

#### 7.3.22.8 Hardware Lock Detection Current Limit (HW\_LOCK\_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The output of current sense amplifier is connected to hardware comparator. If at any time, the voltage on the output of CSA exceeds HW\_LOCK\_ILIMIT threshold for a time longer than  $t_{\text{HW\_LOCK\_ILIMIT}}$ , a HW\_LOCK\_ILIMIT event is recognized and action is taken according to the HW\_LOCK\_ILIMIT\_MODE. The threshold is set through HW\_LOCK\_ILIMIT, the  $t_{\text{HW\_LCK\_ILIMIT}}$  is set through the HW\_LOCK\_ILIMIT\_DEG. HW\_LOCK\_ILIMIT\_MODE bit can operate in four different modes: HW\_LOCK\_ILIMIT latched shutdown, HW\_LOCK\_ILIMIT automatic retry, HW\_LOCK\_ILIMIT report only, and HW\_LOCK\_ILIMIT disabled.

##### 7.3.22.8.1 HW\_LOCK\_ILIMIT Latched Shutdown (HW\_LOCK\_ILIMIT\_MODE = 00xxb)

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFETs during HW\_LOCK\_ILIMIT:



- HW\_LOCK\_ILIMIT\_MODE = 0000b: All MOSFETs are turned OFF.
- HW\_LOCK\_ILIMIT\_MODE = 0001b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- HW\_LOCK\_ILIMIT\_MODE = 0010b: All-high side MOSFETs are turned ON.
- HW\_LOCK\_ILIMIT\_MODE = 0011b: All-low side MOSFETs are turned ON.

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.8.2 HW\_LOCK\_ILIMIT Automatic recovery (HW\_LOCK\_ILIMIT\_MODE = 01xxb)

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFET during HW\_LOCK\_ILIMIT:

- HW\_LOCK\_ILIMIT\_MODE = 0100b: All MOSFETs are turned OFF.
- HW\_LOCK\_ILIMIT\_MODE = 0101b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- HW\_LOCK\_ILIMIT\_MODE = 0110b: All high-side MOSFETs are turned ON
- HW\_LOCK\_ILIMIT\_MODE = 0111b: All low-side MOSFETs are turned ON

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.22.8.3 HW\_LOCK\_ILIMIT Report Only (HW\_LOCK\_ILIMIT\_MODE = 1000b)

No protective action is taken when a HW\_LOCK\_ILIMIT event happens in this mode. The hardware lock detection current limit event is reported by setting the CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits to 1b in the fault status registers. If ALARM\_PIN\_DIS is set to 0b, nFAULT is driven low to report the fault. If ALARM\_PIN\_DIS is set to 1b, nFAULT is not driven low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.8.4 HW\_LOCK\_ILIMIT Disabled (HW\_LOCK\_ILIMIT\_MODE= 1xx1b)

No action is taken when a HW\_LOCK\_ILIMIT event happens in this mode.

#### 7.3.22.9 Thermal Warning (OTW)

If the die temperature exceeds the thermal warning limit ( $T_{OTW}$ ), the OT and OTW bits in the status register are set to 1b. The reporting of OTW on the nFAULT pin can be enabled by setting OTW\_REP to 1b. The device performs no additional action and continues to function. In this case, the nFAULT pin is released when the die temperature decreases below the hysteresis point of the thermal warning limit ( $T_{OTW} - T_{OTW\_HYS}$ ). The OTW bit remains set until cleared through the CLR\_FLT bit and the die temperature is lower than thermal warning limit. ( $T_{OTW}$ ).

---

#### 备注

Over-temperature warning (OTW) is not reported on nFAULT pin by default.

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#### 7.3.22.10 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown limit ( $T_{TSD}$ ), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the DRIVER\_FAULT, OT and TSD bit in the status register are set to 1b. Normal operation resumes (driver operation and the nFAULT pin is released) when the die temperature decreases below the hysteresis point of the thermal shutdown limit ( $T_{TSD} - T_{TSD\_HYS}$ ). The TSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR\_FLT bit. This protection feature cannot be disabled.

### 7.3.22.11 Motor Lock (MTR\_LCK)

The MCF8316A continuously checks for different motor lock conditions (see [Motor Lock Detection](#)) during motor operation. When one of the enabled lock condition happens, a MTR\_LCK event is recognized and action is taken according to the MTR\_LCK\_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK\_RETRY . MTR\_LCK\_MODE bit can operate in four different modes: MTR\_LCK latched shutdown, MTR\_LCK automatic retry, MTR\_LCK report only and MTR\_LCK disabled.

#### 7.3.22.11.1 MTR\_LCK Latched Shutdown (MTR\_LCK\_MODE = 00xxb)

When a MTR\_LCK event happens in this mode, the status of MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of MOSFETs during MTR\_LCK:

- MTR\_LCK\_MODE = 0000b: All MOSFETs are turned OFF.
- MTR\_LCK\_MODE = 0001b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- MTR\_LCK\_MODE = 0010b: All high-side MOSFETs are turned ON.
- MTR\_LCK\_MODE = 0011b: All low-side MOSFETs are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.11.2 MTR\_LCK Automatic Recovery (MTR\_LCK\_MODE= 01xxb)

When a MTR\_LCK event happens in this mode, the status of MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of MOSFETs during MTR\_LCK:

- MTR\_LCK\_MODE = 0100b: All MOSFETs are turned OFF.
- MTR\_LCK\_MODE = 0101b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- MTR\_LCK\_MODE = 0110b: All high-side MOSFETs are turned ON.
- MTR\_LCK\_MODE = 0111b: All low-side MOSFETs are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.22.11.3 MTR\_LCK Report Only (MTR\_LCK\_MODE = 1000b)

No protective action is taken when a MTR\_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits to 1b in the fault status registers. If ALARM\_PIN\_DIS is set to 0b, nFAULT is driven low to report the fault. If ALARM\_PIN\_DIS is set to 1b, nFAULT is not driven low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.11.4 MTR\_LCK Disabled (MTR\_LCK\_MODE = 1xx1b)

No action is taken when a MTR\_LCK event happens in this mode.

### 7.3.22.12 Motor Lock Detection

The MCF8316A provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8316A can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits (LOCK1/2/3\_EN).

### 7.3.22.12.1 Lock 1: Abnormal Speed (ABN\_SPEED)

MCF8316A monitors the speed continuously and at any time the speed exceeds LOCK\_ABN\_SPEED, an ABN\_SPEED lock event is recognized and action is taken according to the MTR\_LCK\_MODE.

The threshold is set through the LOCK\_ABN\_SPEED register. ABN\_SPEED lock can be enabled/disabled by LOCK1\_EN.

### 7.3.22.12.2 Lock 2: Abnormal BEMF (ABN\_BEMF)

MCF8316A estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL\_BEMF\_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR\_LCK\_MODE.

ABN\_BEMF lock can be enabled/disabled by LOCK2\_EN.

### 7.3.22.12.3 Lock3: No-Motor Fault (NO\_MTR)

The MCF8316A continuously monitors phase currents on all three phases; if any phase current stays below NO\_MTR\_THR for 500ms, a NO\_MTR event is recognized. The response to the NO\_MTR event is configured through MTR\_LCK\_MODE. NO\_MTR lock can be enabled/disabled by LOCK3\_EN.

### 7.3.22.13 MPET Faults

An error during resistance and inductance measurement is reported using MPET\_IPD\_FAULT. The MPET\_IPD\_FAULT gets triggered when the IPD timer overflows due to unsuccessful attempt to ramp up the current to the threshold value, same as explained in [节 7.3.22.14](#). The fault typically gets triggered when there is no motor connected to MCF8316 or when the MPET IPD current threshold is set high for motors with high resistance.

An error during BEMF constant measurement is reported using MPET\_BEMF\_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT\_DETECT\_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

### 7.3.22.14 IPD Faults

The MCF8316A uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR\_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD\_CURR\_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD\_CURR\_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD\_CURR\_THR) with all the four clock frequencies, then the IPD\_T1\_FAULT gets triggered. Similarly the algorithm check sfor a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD\_T2\_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD\_TIMEOUT\_FAULT\_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8316A can generate a fault called IPD\_FREQ\_FAULT during such a scenario by setting IPD\_FREQ\_FAULT\_EN to 1b. The IPD\_FREQ\_FAULT maybe triggerd if the IPD frequency is too high for the IPD current limit and the IPD release mode or if the motor inductance is too high for the IPD frequency, IPD current limit and IPD release mode.

## 7.4 Device Functional Modes

### 7.4.1 Functional Modes

#### 7.4.1.1 Sleep Mode

In sleep mode, the MOSFETs, sense amplifiers, buck regulator, charge pump, AVDD LDO regulator and the I<sup>2</sup>C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV\_MODE to 1b. SPEED pin determines entry and exit from sleep state as described in [表 7-6](#).

#### 备注

During power-up and power-down of the device, the nFAULT pin is held low as the internal regulators are disabled. After the regulators have been enabled, the nFAULT pin is automatically released.

#### 7.4.1.2 Standby Mode

In standby mode the charge pump, AVDD LDO, buck regulator and I<sup>2</sup>C bus are active. The device can be configured to enter standby mode by configuring DEV\_MODE to 0b. SPEED pin determines entry and exit from standby state as described in [表 7-6](#)

#### 7.4.1.3 Fault Reset (CLR\_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR\_FLT to 1b.

**表 7-6. Conditions to Enter or Exit Sleep or Standby Modes**

| SPEED COMMAND MODE | ENTER STANDBY CONDITION   | ENTER SLEEP CONDITION   | EXIT FROM STANDBY CONDITION  | EXIT FROM SLEEP CONDITION  |
|--------------------|---|---|--|--|
| Analog             | SPEED pin voltage < V <sub>EN_SB</sub> for t <sub>DET_SB_ANA</sub>                            | SPEED pin voltage < V <sub>EN_SL</sub> for t <sub>DET_SL_ANA</sub>                              | SPEED pin voltage > V <sub>EX_SB</sub> for t <sub>DET_ANA</sub>    | SPEED pin voltage > V <sub>EX_SL</sub> for t <sub>DET_ANA</sub>    |
| PWM/<br>Frequency  | SPEED pin low (V < V <sub>DIG_IL</sub> ) for t <sub>EN_SB_PWM</sub> / t <sub>EN_SB_FREQ</sub> | SPEED pin low (V < V <sub>DIG_IL</sub> ) for t <sub>DET_SL_PWM</sub> / t <sub>DET_SL_FREQ</sub> | SPEED pin high (V > V <sub>DIG_IH</sub> ) for t <sub>DET_PWM</sub> | SPEED pin high (V > V <sub>DIG_IH</sub> ) for t <sub>DET_PWM</sub> |
| I <sup>2</sup> C   | DIGITAL_SPEED_CTRL is programmed as 0.  | SPEED pin voltage < V <sub>EN_SL</sub> for t > SLEEP_ENTRY_TIME                                 | DIGITAL_SPEED_CTRL is programmed as non-zero.                      | SPEED pin voltage > V <sub>EX_SL</sub> for t <sub>DET_ANA</sub>    |

## 7.5 External Interface

### 7.5.1 DRVOFF Functionality

When DRVOFF pin is driven high, all six MOSFETs are disabled. In this mode, if SPEED pin is high, the charge pump, AVDD regulator, buck regulator and I<sup>2</sup>C bus are active; driver faults like OCP will be inactive.

### 7.5.2 SOX Output

MCF8316A can provide the built-in current sense amplifiers' output on the SOX pin. SOX output is available on pin 38 and can be configured by PIN\_38\_CONFIG

### 7.5.3 Oscillator Source

MCF8316A has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8316A is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCF8316A does not meet accuracy requirements of timing measurement or speed loop, then MCF8316A has an option to support an external clock reference.

In order to improve EMI performance, MCF8316A provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD\_SPECTRUM\_MODULATION\_DIS

### 7.5.3.1 External Clock Source

Speed loop accuracy of MCF8316A over wide operating temperature range can be improved by providing more accurate optional clock reference on EXT\_CLK pin as shown in 图 7-52. EXT\_CLK will be used to calibrate internal clock oscillator and match the accuracy of the external clock. External clock source can be selected by configuring CLK\_SEL to 11b and setting EXT\_CLK\_EN to 1b. The external clock source frequency can be configured through EXT\_CLK\_CONFIG.

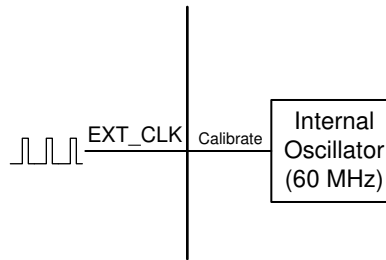


图 7-52. External Clock Reference

#### 备注

External clock is optional and can be used when higher clock accuracy is needed. MCF8316A will always power up using the internal oscillator in all modes.

### 7.5.4 External Watchdog

MCF8316A provides an external watchdog feature - EXT\_WD\_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in GPIO mode, WATCHDOG\_TICKLE set to 1b in I<sup>2</sup>C mode) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is higher than the configured time, a watchdog fault is triggered. This fault can be configured using EXT\_WD\_FAULT either as a report only fault or as a latched fault with outputs in Hi-Z state. The latched fault can be cleared by writing 1b to CLR\_FLT. In case, the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously monitor the health of an external MCU (which is the external watchdog input) and put the MCF8316A outputs in Hi-Z in case the external MCU is in an erroneous state.

The external watchdog input is selected using EXT\_WD\_INPUT and can either be the EXT\_WD pin or the I<sup>2</sup>C interface. The time interval between two tickles to trigger a watchdog fault is configured by EXT\_WD\_CONFIG; there are 4 time settings - 100, 200, 500 and 1000ms for the EXT\_WD pin based watchdog and 4 time settings - 1, 2, 5 and 10s for the I<sup>2</sup>C based watchdog.

## 7.6 EEPROM access and I<sup>2</sup>C interface

### 7.6.1 EEPROM Access

MCF8316A has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I<sup>2</sup>C serial interface but erase cannot be performed using I<sup>2</sup>C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

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#### 备注

MCF8316A allows EEPROM write and read operations only when the motor is not spinning.

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#### 7.6.1.1 EEPROM Write

In MCF8316A, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD\_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV\_DRIVE\_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084 (MOTOR\_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR\_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED\_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A (CLOSED\_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED\_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E (CLOSED\_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090 (FAULT\_CONFIG1) with fault control configuration software and hardware current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092 (FAULT\_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED\_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT\_ALGO\_1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2 (INT\_ALGO\_2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN\_CONFIG1) with pin configuration for speed input mode (analog or PWM), BRAKE pin mode etc.
15. Write registers 0x0000A6 and 0x0000A8 (DEVICE\_CONFIG1 and DEVICE\_CONFIG2) with device configuration like pins 36, 37 configuration, pin 38 configuration, dynamic CSA gain enable, dynamic voltage gain enable, clock source select, speed range select etc.
16. Write register 0x0000AA (PERI\_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD\_CONFIG1 and GD\_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 100ms for the EEPROM write operation to complete

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 18 should be executed to copy the contents of the shadow registers into the EEPROM.

### 7.6.1.2 EEPROM Read

In MCF8316A, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values, 1 or 2 registers at a time, using the I<sup>2</sup>C read command as explained in [节 7.6.2](#). Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

### 7.6.2 I<sup>2</sup>C Serial Interface

MCF8316A interfaces with an external MCU over an I<sup>2</sup>C serial interface. MCF8316A is an I<sup>2</sup>C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8316A

#### 备注

For reliable communication, a 100- $\mu$ s delay should be used between every byte transferred over the I<sup>2</sup>C bus.

#### 7.6.2.1 I<sup>2</sup>C Data Word

The I<sup>2</sup>C data word format is shown in [表 7-7](#).

表 7-7. I<sup>2</sup>C Data Word Format

| TARGET_ID | R/W | CONTROL WORD | DATA                | CRC-8   |
|-----------|-----|--------------|---------------------|---------|
| A6 - A0   | W0  | CW23 - CW0   | D15 / D31/ D63 - D0 | C7 - C0 |

**Target ID and R/W Bit:** The first byte includes the 7-bit I<sup>2</sup>C target ID (0x01), followed by the read/write command bit. Every packet in MCF8316A the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

**24-bit Control Word:** The Target Address is followed by a 24-bit control bit. The control word format is shown in [表 7-8](#).

表 7-8. 24-bit Control Word Format

| OP_R/W | CRC_EN | DLEN       | MEM_SEC     | MEM_PAGE    | MEM_ADDR   |
|--------|--------|------------|-------------|-------------|------------|
| CW23   | CW22   | CW21- CW20 | CW19 - CW16 | CW15 - CW12 | CW11 - CW0 |

Each field in the control word is explained in detail below.

**OP\_R/W – Read/Write:** R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCF8316A will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8316A will expect an I<sup>2</sup>C read request with repeated start or normal start after the 24-bit control word.

**CRC\_EN – Cyclic Redundancy Check(CRC) Enable:** MCF8316A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

**DLEN – Data Length:** DLEN field determines the length of the data that will be sent by external MCU to MCF8316A. MCF8316A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

表 7-9. Data Length Configuration

| DLEN Value | Data Length |
|------------|-------------|
| 00b        | 16-bit      |

表 7-9. Data Length Configuration (continued)

| DLEN Value | Data Length |
|------------|-------------|
| 01b        | 32-bit      |
| 10b        | 64-bit      |
| 11b        | Reserved    |

**MEM\_SEC – Memory Section:** Each memory location in MCF8316A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

**MEM\_PAGE – Memory Page:** Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

**MEM\_ADDR – Memory Address:** Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8316A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800)

**Data Bytes:** For a write operation to MCF8316A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

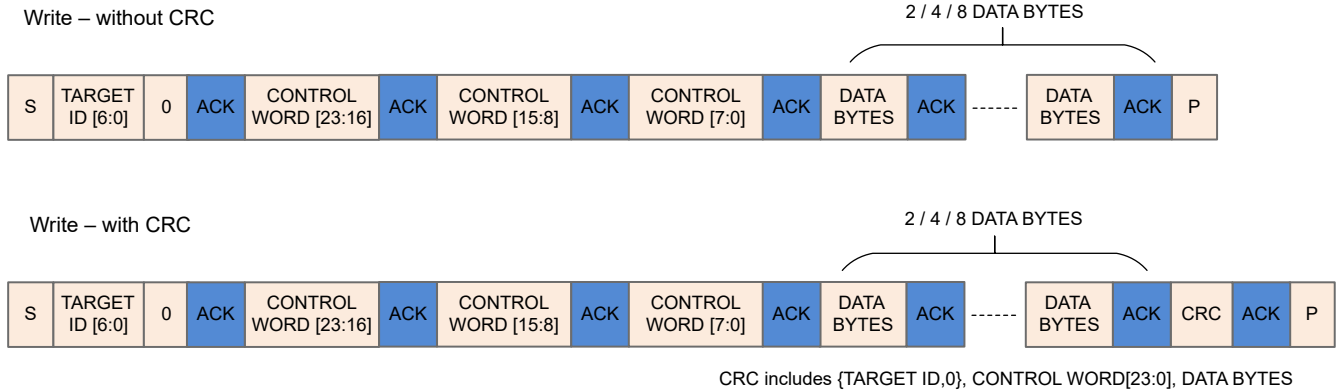
**CRC Byte:** If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

#### 7.6.2.2 I<sup>2</sup>C Write Operation

MCF8316A write operation over I<sup>2</sup>C involves the following sequence.

1. I<sup>2</sup>C start condition.
2. The sequence starts with I<sup>2</sup>C target start byte, made up of 7-bit target ID (0x01) to identify the MCF8316A along with the R/W bit set to 0.
3. The start byte is followed by 24-bit control word. Bit 23 in the control word has to be 0 as it is a write operation.
4. The 24-bit control word is then followed by the data bytes. The length of the data byte depends on the DLEN field.
  - a. While sending data bytes, the LSB byte is sent first. Refer below examples for more details.
  - b. 16-bit/32-bit write – The data sent is written to the address mentioned in Control Word.
  - c. 64-bit Write – 64-bit is treated as two 32-bit writes. The address mentioned in Control word is taken as Addr 0. Addr 1 is calculating internally by MCF8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first way) are written to Addr 0 and the next 4 bytes are written to Addr 1.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes).
6. I<sup>2</sup>C stop condition.



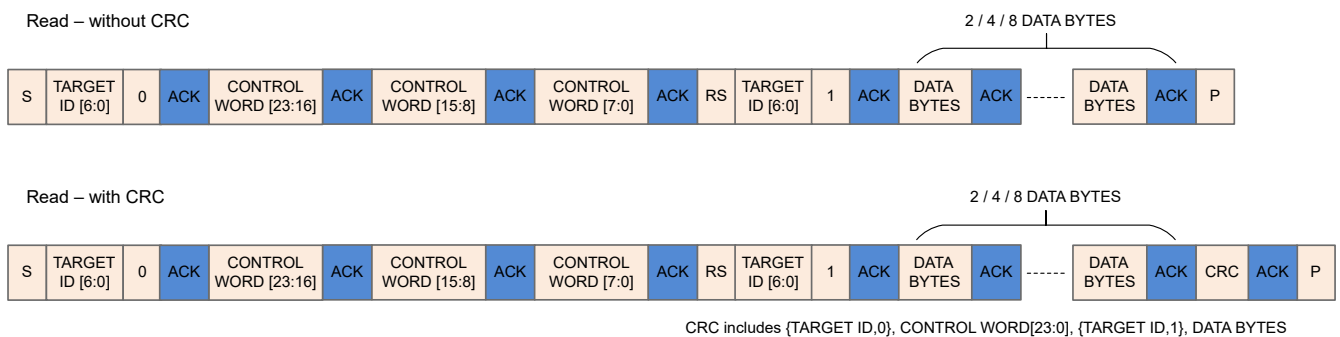


**图 7-53. I<sup>2</sup>C Write Operation Sequence**

### 7.6.2.3 I<sup>2</sup>C Read Operation

MCF8316A read operation over I<sup>2</sup>C involves the following sequence.

1. I<sup>2</sup>C start condition.
2. The sequence starts with I<sup>2</sup>C target Start Byte.
3. The Start Byte is followed by 24-bit Control Word. Bit 23 in the control word has to be 1 as it is a read operation.
4. The control word is followed by a repeated start or normal start.
5. MCF8316A sends the data bytes on SDA. The number of bytes sent by MCF8316A depends on the DLEN field value in the control word.
  - a. While sending data bytes, the LSB byte is sent first. Refer the examples below for more details.
  - b. 16-bit/32-bit Read – The data from the address mentioned in Control Word is sent back.
  - c. 64-bit Read – 64-bit is treated as two 32-bit read. The address mentioned in Control Word is taken as Addr 0. Addr 1 is calculating internally by MCF8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent by MCF8316A. The first 4 bytes (sent in LSB first way) are read from Addr 0 and the next 4 bytes are read from Addr 1.
  - d. MCF8316A takes some time to process the control word and read data from the given address. This involves some delay. It is quite possible that the repeated start with Target ID will be NACK'd. If the I<sup>2</sup>C read request has been NACK'd by MCF8316A, retry after few cycles. During this retry, it is not necessary to send the entire packet along with the control word. It is sufficient to send only the start condition with target ID and read bit.
6. If CRC is enabled, then MCF8316A sends an additional CRC byte at the end. If CRC is enabled, external MCU I<sup>2</sup>C controller has to read this additional byte before sending the stop bit. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I<sup>2</sup>C stop condition.



**图 7-54. I<sup>2</sup>C Read Operation Sequence**

### 7.6.2.4 Examples of MCF8316A I<sup>2</sup>C Communication Protocol Packets

All values used in this example section are in hex format. I<sup>2</sup>C target ID used in the examples is 0x01.

**Example for 32-bit Write Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

**表 7-10. Example for 32-bit Write Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 |          | Control Word 2 | Data Bytes |       |       |       | CRC      |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------|----------------|------------|-------|-------|-------|----------|
| Target ID  | I <sup>2</sup> C Write | OP_R/W         | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR | MEM_ADDR       | DB0        | DB1   | DB2   | DB3   | CRC Byte |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8 | CW7-CW0        | D7-D0      | D7-D0 | D7-D0 | D7-D0 | C7-C0    |
| 0x01       | 0x0                    | 0x0            | 0x1    | 0x1       | 0x0       | 0x0            | 0x0      | 0x80           | 0xCD       | 0xAB  | 0x34  | 0x12  | 0x45     |
| 0x02       |                        | 0x50           |        |           |           | 0x00           |          | 0x80           | 0xCD       | 0xAB  | 0x34  | 0x12  | 0x45     |

**Example for 64-bit Write Operation:** Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

**表 7-11. Example for 64-bit Write Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 |          | Control Word 2 | Data Bytes        | CRC      |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------|----------------|-------------------|----------|
| Target ID  | I <sup>2</sup> C Write | OP_R/W         | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR | MEM_ADDR       | DB0 - DB7         | CRC Byte |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8 | CW7-CW0        | [D7-D0] x 8       | C7-C0    |
| 0x01       | 0x0                    | 0x0            | 0x1    | 0x2       | 0x0       | 0x0            | 0x0      | 0x80           | 0x67452301EFCDA89 | 0x45     |
| 0x02       |                        | 0x60           |        |           |           | 0x00           |          | 0x80           | 0x67452301EFCDA89 | 0x45     |

**Example for 32-bit Read Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

**表 7-12. Example for 32-bit Read Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 |          | Control Word 2 | Start Byte | Byte 0                | Byte 1 | Byte 2 | Byte 3 | Byte 4 |          |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------|----------------|------------|-----------------------|--------|--------|--------|--------|----------|
| Target ID  | I <sup>2</sup> C Write | R/W            | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR | MEM_ADDR       | Target ID  | I <sup>2</sup> C Read | DB0    | DB1    | DB2    | DB3    | CRC Byte |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8 | CW7-CW0        | A6-A0      | W0                    | D7-D0  | D7-D0  | D7-D0  | D7-D0  | C7-C0    |
| 0x01       | 0x0                    | 0x1            | 0x1    | 0x1       | 0x0       | 0x0            | 0x0      | 0x80           | 0x01       | 0x1                   | 0xCD   | 0xAB   | 0x34   | 0x12   | 0x56     |
| 0x02       |                        | 0xD0           |        |           |           | 0x00           |          | 0x80           | 0x03       |                       | 0xCD   | 0xAB   | 0x34   | 0x12   | 0x56     |

### 7.6.2.5 Internal Buffers

MCF8316A uses buffers internally to store the data received on I<sup>2</sup>C. Highest priority is given to collecting data on the I<sup>2</sup>C Bus. There are 2 buffers (ping-pong) for I<sup>2</sup>C Rx Data and 2 buffers (ping-pong) for I<sup>2</sup>C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCF8316A is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I<sup>2</sup>C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCF8316A can accommodate a maximum of two consecutive read/write requests. If MCF8316A is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK'd as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I<sup>2</sup>C Read (Target ID + R bit), the data from this Tx Buffer is sent over I<sup>2</sup>C. Since there are two Tx Buffers, register data from 2 MCF8316A reads

can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCF8316A as the Tx Buffers are full.

Once a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I<sup>2</sup>C read (only I<sup>2</sup>C read, without any control word information) to read all the data bytes from first.

#### **7.6.2.6 CRC Byte Calculation**

An 8-bit CCIT polynomial ( $x^8 + x^2 + x + 1$ ) is used for CRC computation.

**CRC Calculation in Write Operation:** When the external MCU writes to MCF8316A, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8316A will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

**CRC Calculation in Read Operation:** When the external MCU reads from MCF8316A, if the CRC is enabled, MCF8316A sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8316A. Input data for CRC calculation by external MCU to verify the data sent by MCF8316A are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

## 7.7 EEPROM (Non-Volatile) Register Map

### 7.7.1 Algorithm\_Configuration Registers

[ALGORITHM\\_CONFIGURATION Registers](#) lists the memory-mapped registers for the Algorithm\_Configuration registers. All register offset addresses not listed in [ALGORITHM\\_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

**表 7-13. ALGORITHM\_CONFIGURATION Registers**

| Address | Acronym          | Register Name                 | Section                    |
|---------|------------------|-------------------------------|----------------------------|
| 80h     | ISD_CONFIG       | ISD Configuration             | <a href="#">节 7.7.1.1</a>  |
| 82h     | REV_DRIVE_CONFIG | Reverse Drive Configuration   | <a href="#">节 7.7.1.2</a>  |
| 84h     | MOTOR_STARTUP1   | Motor Startup Configuration 1 | <a href="#">节 7.7.1.3</a>  |
| 86h     | MOTOR_STARTUP2   | Motor Startup Configuration 2 | <a href="#">节 7.7.1.4</a>  |
| 88h     | CLOSED_LOOP1     | Closed Loop Configuration 1   | <a href="#">节 7.7.1.5</a>  |
| 8Ah     | CLOSED_LOOP2     | Closed Loop Configuration 2   | <a href="#">节 7.7.1.6</a>  |
| 8Ch     | CLOSED_LOOP3     | Closed Loop Configuration 3   | <a href="#">节 7.7.1.7</a>  |
| 8Eh     | CLOSED_LOOP4     | Closed Loop Configuration 4   | <a href="#">节 7.7.1.8</a>  |
| 94h     | SPEED_PROFILES1  | Speed Profile Configuration 1 | <a href="#">节 7.7.1.9</a>  |
| 96h     | SPEED_PROFILES2  | Speed Profile Configuration 2 | <a href="#">节 7.7.1.10</a> |
| 98h     | SPEED_PROFILES3  | Speed Profile Configuration 3 | <a href="#">节 7.7.1.11</a> |
| 9Ah     | SPEED_PROFILES4  | Speed Profile Configuration 4 | <a href="#">节 7.7.1.12</a> |
| 9Ch     | SPEED_PROFILES5  | Speed Profile Configuration 5 | <a href="#">节 7.7.1.13</a> |
| 9Eh     | SPEED_PROFILES6  | Speed Profile Configuration 6 | <a href="#">节 7.7.1.14</a> |

Complex bit access types are encoded to fit into small table cells. [Algorithm\\_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

**表 7-14. Algorithm\_Configuration Access Type Codes**

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Write Type</b>             |      |  |
| W                             | W    | Write                                  |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

### 7.7.1.1 ISD\_CONFIG Register (Address = 80h) [Reset = 0000000h]

ISD\_CONFIG is shown in [ISD\\_CONFIG Register](#) and described in [ISD\\_CONFIG Register Field Descriptions](#).  
Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure initial speed detect settings

**图 7-55. ISD\_CONFIG Register**

|                  |  |        |  |                     |  |        |  |           |  |           |  |                           |  |    |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
|------------------|--|--------|--|---------------------|--|--------|--|-----------|--|-----------|--|---------------------------|--|----|--|-----------------|--|--|--|----|--|--|--|----|--|--|--|----|--|--|--|
| 31               |  | 30     |  | 29                  |  | 28     |  | 27        |  | 26        |  | 25                        |  | 24 |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| PARITY           |  | ISD_EN |  | BRAKE_EN            |  | HIZ_EN |  | RVS_DR_EN |  | RESYNC_EN |  | FW_DRV_RESYN_THR          |  |    |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| R/W-0h           |  | R/W-0h |  | R/W-0h              |  | R/W-0h |  | R/W-0h    |  | R/W-0h    |  | R/W-0h                    |  |    |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| 23               |  |        |  | 22                  |  |        |  | 21        |  |           |  | 20                        |  |    |  | 19              |  |  |  | 18 |  |  |  | 17 |  |  |  | 16 |  |  |  |
| FW_DRV_RESYN_THR |  |        |  | BRK_MODE            |  |        |  | RESERVED  |  |           |  | RESERVED                  |  |    |  | BRK_TIME        |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| R/W-0h           |  |        |  | R/W-0h              |  |        |  | R/W-0h    |  |           |  | R/W-0h                    |  |    |  | R/W-0h          |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| 15               |  |        |  | 14                  |  |        |  | 13        |  |           |  | 12                        |  |    |  | 11              |  |  |  | 10 |  |  |  | 9  |  |  |  | 8  |  |  |  |
| BRK_TIME         |  |        |  |                     |  |        |  | HIZ_TIME  |  |           |  |                           |  |    |  | STAT_DETECT_THR |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| R/W-0h           |  |        |  |                     |  |        |  | R/W-0h    |  |           |  |                           |  |    |  | R/W-0h          |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| 7                |  |        |  | 6                   |  |        |  | 5         |  |           |  | 4                         |  |    |  | 3               |  |  |  | 2  |  |  |  | 1  |  |  |  | 0  |  |  |  |
| STAT_DETECT_THR  |  |        |  | REV_DRV_HANDOFF_THR |  |        |  |           |  |           |  | REV_DRV_OPEN_LOOP_CURRENT |  |    |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |
| R/W-0h           |  |        |  | R/W-0h              |  |        |  |           |  |           |  | R/W-0h                    |  |    |  |                 |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |

**表 7-15. ISD\_CONFIG Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 31  | PARITY    | R/W  | 0h    | Parity bit  |
| 30  | ISD_EN    | R/W  | 0h    | ISD enable<br>0h = Disable<br>1h = Enable               |
| 29  | BRAKE_EN  | R/W  | 0h    | Brake enable<br>0h = Disable<br>1h = Enable             |
| 28  | HIZ_EN    | R/W  | 0h    | Hi-Z enable<br>0h = Disable<br>1h = Enable              |
| 27  | RVS_DR_EN | R/W  | 0h    | Reverse drive enable<br>0h = Disable<br>1h = Enable     |
| 26  | RESYNC_EN | R/W  | 0h    | Resynchronization enable<br>0h = Disable<br>1h = Enable |

表 7-15. ISD\_CONFIG Register Field Descriptions (continued)

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 25-22 | FW_DRV_RESYN_THR | R/W  | 0h    | Minimum speed threshold to resynchronize to close loop (% of MAX_SPEED)<br>0h = 5%<br>1h = 10%<br>2h = 15%<br>3h = 20%<br>4h = 25%<br>5h = 30%<br>6h = 35%<br>7h = 40%<br>8h = 45%<br>9h = 50%<br>Ah = 55%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 21    | BRK_MODE         | R/W  | 0h    | Brake mode<br>0h = All three high side FETs turned ON<br>1h = All three low side FETs turned ON   |
| 20    | RESERVED         | R/W  | 0h    | Reserved  |
| 19-17 | RESERVED         | R/W  | 0h    | Reserved  |
| 16-13 | BRK_TIME         | R/W  | 0h    | Brake time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 2 s<br>Ah = 3 s<br>Bh = 4 s<br>Ch = 5 s<br>Dh = 7.5 s<br>Eh = 10 s<br>Fh = 15 s                                    |

**表 7-15. ISD\_CONFIG Register Field Descriptions (continued)**

| Bit  | Field                     | Type | Reset | Description  |
|------|---------------------------|------|-------|--|
| 12-9 | HIZ_TIME                  | R/W  | 0h    | Hi-Z time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 2 s<br>Ah = 3 s<br>Bh = 4 s<br>Ch = 5 s<br>Dh = 7.5 s<br>Eh = 10 s<br>Fh = 15 s  |
| 8-6  | STAT_DETECT_THR           | R/W  | 0h    | BEMF threshold to detect if motor is stationary<br>0h = 50 mV<br>1h = 75 mV<br>2h = 100 mV<br>3h = 250 mV<br>4h = 500 mV<br>5h = 750 mV<br>6h = 1000 mV<br>7h = 1500 mV  |
| 5-2  | REV_DRV_HANDOFF_THR       | R/W  | 0h    | Speed threshold used to transition to open loop during reverse deceleration (% of MAX_SPEED)<br>0h = 2.5%<br>1h = 5%<br>2h = 7.5%<br>3h = 10%<br>4h = 12.5%<br>5h = 15%<br>6h = 20%<br>7h = 25%<br>8h = 30%<br>9h = 40%<br>Ah = 50%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 1-0  | REV_DRV_OPEN_LOOP_CURRENT | R/W  | 0h    | Open loop current limit during speed reversal<br>0h = 1.5 A<br>1h = 2.5 A<br>2h = 3.5 A<br>3h = 5.0 A  |

**7.7.1.2 REV\_DRIVE\_CONFIG Register (Address = 82h) [Reset = 0000000h]**

REV\_DRIVE\_CONFIG is shown in [REV\\_DRIVE\\_CONFIG Register](#) and described in [REV\\_DRIVE\\_CONFIG Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure reverse drive settings

**图 7-56. REV\_DRIVE\_CONFIG Register**

|                            |                            |        |    |                            |                 |    |    |
|----------------------------|----------------------------|--------|----|----------------------------|-----------------|----|----|
| 31                         | 30                         | 29     | 28 | 27                         | 26              | 25 | 24 |
| PARITY                     | REV_DRV_OPEN_LOOP_ACCEL_A1 |        |    | REV_DRV_OPEN_LOOP_ACCEL_A2 |                 |    |    |
| R/W-0h                     |                            | R/W-0h |    |                            | R/W-0h          |    |    |
| 23                         | 22                         | 21     | 20 | 19                         | 18              | 17 | 16 |
| REV_DRV_OPEN_LOOP_ACCEL_A2 | ACTIVE_BRAKE_CURRENT_LIMIT |        |    | ACTIVE_BRAKE_KP            |                 |    |    |
| R/W-0h                     |                            | R/W-0h |    |                            | R/W-0h          |    |    |
| 15                         | 14                         | 13     | 12 | 11                         | 10              | 9  | 8  |
| ACTIVE_BRAKE_KP            |                            |        |    |                            | ACTIVE_BRAKE_KI |    |    |
| R/W-0h                     |                            |        |    | R/W-0h                     |                 |    |    |
| 7                          | 6                          | 5      | 4  | 3                          | 2               | 1  | 0  |
| ACTIVE_BRAKE_KI            |                            |        |    |                            |                 |    |    |
| R/W-0h                     |                            |        |    |                            |                 |    |    |

**表 7-16. REV\_DRIVE\_CONFIG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description  |
|-------|----------------------------|------|-------|--|
| 31    | PARITY                     | R/W  | 0h    | Parity bit   |
| 30-27 | REV_DRV_OPEN_LOOP_ACCEL_A1 | R/W  | 0h    | Open loop acceleration coefficient A1 during reverse drive<br>0h = 0.01 Hz/s<br>1h = 0.05 Hz/s<br>2h = 1 Hz/s<br>3h = 2.5 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 25 Hz/s<br>7h = 50 Hz/s<br>8h = 75 Hz/s<br>9h = 100 Hz/s<br>Ah = 250 Hz/s<br>Bh = 500 Hz/s<br>Ch = 750 Hz/s<br>Dh = 1000 Hz/s<br>Eh = 5000 Hz/s<br>Fh = 10000 Hz/s |



**表 7-16. REV\_DRIVE\_CONFIG Register Field Descriptions (continued)**

| Bit   | Field                      | Type | Reset | Description   |
|-------|----------------------------|------|-------|---|
| 26-23 | REV_DRV_OPEN_LOOP_ACCEL_A2 | R/W  | 0h    | Open loop acceleration coefficient A2 during reverse drive<br>0h = 0.0 Hz/s <sup>2</sup><br>1h = 0.05 Hz/s <sup>2</sup><br>2h = 1 Hz/s <sup>2</sup><br>3h = 2.5 Hz/s <sup>2</sup><br>4h = 5 Hz/s <sup>2</sup><br>5h = 10 Hz/s <sup>2</sup><br>6h = 25 Hz/s <sup>2</sup><br>7h = 50 Hz/s <sup>2</sup><br>8h = 75 Hz/s <sup>2</sup><br>9h = 100 Hz/s <sup>2</sup><br>Ah = 250 Hz/s <sup>2</sup><br>Bh = 500 Hz/s <sup>2</sup><br>Ch = 750 Hz/s <sup>2</sup><br>Dh = 1000 Hz/s <sup>2</sup><br>Eh = 5000 Hz/s <sup>2</sup><br>Fh = 10000 Hz/s <sup>2</sup> |
| 22-20 | ACTIVE_BRAKE_CURRENT_LIMIT | R/W  | 0h    | Bus current limit during active braking<br>0h = 0.5 A<br>1h = 1 A<br>2h = 2 A<br>3h = 3 A<br>4h = 4 A<br>5h = 5 A<br>6h = 6 A<br>7h = 7 A   |
| 19-10 | ACTIVE_BRAKE_KP            | R/W  | 0h    | 10-bit value for active braking loop Kp. $K_p = \text{ACTIVE\_BRAKE\_KP} / 2^7$   |
| 9-0   | ACTIVE_BRAKE_KI            | R/W  | 0h    | 10-bit value for active braking loop Ki. $K_i = \text{ACTIVE\_BRAKE\_KI} / 2^9$   |

### 7.7.1.3 MOTOR\_STARTUP1 Register (Address = 84h) [Reset = 0000000h]

MOTOR\_STARTUP1 is shown in [MOTOR\\_STARTUP1 Register](#) and described in [MOTOR\\_STARTUP1 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure motor startup settings<sup>1</sup>

**图 7-57. MOTOR\_STARTUP1 Register**

|               |             |                              |                      |                  |            |                 |                |
|---------------|-------------|------------------------------|----------------------|------------------|------------|-----------------|----------------|
| 31            | 30          | 29                           | 28                   | 27               | 26         | 25              | 24             |
| PARITY        | MTR_STARTUP |                              | ALIGN_SLOW_RAMP_RATE |                  |            | ALIGN_TIME      |                |
| R/W-0h        | R/W-0h      |                              | R/W-0h               |                  |            | R/W-0h          |                |
| 23            | 22          | 21                           | 20                   | 19               | 18         | 17              | 16             |
| ALIGN_TIME    |             | ALIGN_OR_SLOW_CURRENT_ILIMIT |                      |                  |            | IPD_CLK_FREQ    |                |
| R/W-0h        |             | R/W-0h                       |                      |                  |            | R/W-0h          |                |
| 15            | 14          | 13                           | 12                   | 11               | 10         | 9               | 8              |
| IPD_CLK_FREQ  |             | IPD_CURR_THR                 |                      |                  |            | IPD_RLS_MODE    |                |
| R/W-0h        |             | R/W-0h                       |                      |                  |            | R/W-0h          |                |
| 7             | 6           | 5                            | 4                    | 3                | 2          | 1               | 0              |
| IPD_ADV_ANGLE |             | IPD_REPEAT                   |                      | OL_ILIMIT_CONFIG | IQ_RAMP_EN | ACTIVE_BRAKE_EN | REV_DRV_CONFIG |
| R/W-0h        |             | R/W-0h                       |                      | R/W-0h           | R/W-0h     | R/W-0h          | R/W-0h         |

**表 7-17. MOTOR\_STARTUP1 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 31    | PARITY               | R/W  | 0h    | Parity bit  |
| 30-29 | MTR_STARTUP          | R/W  | 0h    | Motor start-up method<br>0h = Align<br>1h = Double Align<br>2h = IPD<br>3h = Slow first cycle   |
| 28-25 | ALIGN_SLOW_RAMP_RATE | R/W  | 0h    | Align, slow first cycle and open loop current ramp rate<br>0h = 0.1 A/s<br>1h = 1 A/s<br>2h = 5 A/s<br>3h = 10 A/s<br>4h = 15 A/s<br>5h = 25 A/s<br>6h = 50 A/s<br>7h = 100 A/s<br>8h = 150 A/s<br>9h = 200 A/s<br>Ah = 250 A/s<br>Bh = 500 A/s<br>Ch = 1000 A/s<br>Dh = 2000 A/s<br>Eh = 5000 A/s<br>Fh = No Limit A/s |

**表 7-17. MOTOR\_STARTUP1 Register Field Descriptions (continued)**

| Bit   | Field                        | Type | Reset | Description  |
|-------|------------------------------|------|-------|--|
| 24-21 | ALIGN_TIME                   | R/W  | 0h    | Align time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 1.5 s<br>Ah = 2 s<br>Bh = 3 s<br>Ch = 4 s<br>Dh = 5 s<br>Eh = 7.5 s<br>Fh = 10 s                                      |
| 20-17 | ALIGN_OR_SLOW_CURRENT_ILIMIT | R/W  | 0h    | Align or slow first cycle current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |
| 16-14 | IPD_CLK_FREQ                 | R/W  | 0h    | IPD clock frequency<br>0h = 50 Hz<br>1h = 100 Hz<br>2h = 250 Hz<br>3h = 500 Hz<br>4h = 1000 Hz<br>5h = 2000 Hz<br>6h = 5000 Hz<br>7h = 10000 Hz  |

表 7-17. MOTOR\_STARTUP1 Register Field Descriptions (continued)

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 13-9 | IPD_CURR_THR     | R/W  | 0h    | IPD current threshold<br>0h = 0.25 A<br>1h = 0.5 A<br>2h = 0.75 A<br>3h = 1.0 A<br>4h = 1.25 A<br>5h = 1.5 A<br>6h = 2.0 A<br>7h = 2.5 A<br>8h = 3.0 A<br>9h = 3.667 A<br>Ah = 4.0 A<br>Bh = 4.667 A<br>Ch = 5.0 A<br>Dh = 5.333 A<br>Eh = 6.0 A<br>Fh = 6.667 A<br>10h = 7.333 A<br>11h = 8.0 A<br>12h = NA<br>13h = NA<br>14h = NA<br>15h = NA<br>16h = NA<br>17h = NA<br>18h = NA<br>19h = NA<br>1Ah = NA<br>1Bh = NA<br>1Ch = NA<br>1Dh = NA<br>1Eh = NA<br>1Fh = NA |
| 8    | IPD_RLS_MODE     | R/W  | 0h    | IPD release mode<br>0h = Brake<br>1h = Tristate  |
| 7-6  | IPD_ADV_ANGLE    | R/W  | 0h    | IPD advance angle<br>0h = 0°<br>1h = 30°<br>2h = 60°<br>3h = 90°   |
| 5-4  | IPD_REPEAT       | R/W  | 0h    | Number of times IPD is executed<br>0h = 1 time<br>1h = average of 2 times<br>2h = average of 3 times<br>3h = average of 4 times  |
| 3    | OL_ILIMIT_CONFIG | R/W  | 0h    | Open loop current limit configuration<br>0h = Open loop current limit defined by OL_ILIMIT<br>1h = Open loop current limit defined by ILIMIT   |
| 2    | IQ_RAMP_EN       | R/W  | 0h    | Iq ramp down before transition to close loop<br>0h = Disable Iq ramp down<br>1h = Enable Iq ramp down  |

**表 7-17. MOTOR\_STARTUP1 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 1   | ACTIVE_BRAKE_EN | R/W  | 0h    | Active braking enable<br>0h = Disable Active Brake<br>1h = Enable Active Brake  |
| 0   | REV_DRV_CONFIG  | R/W  | 0h    | Chooses between forward and reverse drive setting for reverse drive<br>0h = Open loop current, A1, A2 based on forward drive<br>1h = Open loop current, A1, A2 based on reverse drive |

**7.7.1.4 MOTOR\_STARTUP2 Register (Address = 86h) [Reset = 0000000h]**

MOTOR\_STARTUP2 is shown in [MOTOR\\_STARTUP2 Register](#) and described in [MOTOR\\_STARTUP2 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure motor startup settings2

**图 7-58. MOTOR\_STARTUP2 Register**

|                     |           |        |             |                      |                       |        |        |
|---------------------|-----------|--------|-------------|----------------------|-----------------------|--------|--------|
| 31                  | 30        | 29     | 28          | 27                   | 26                    | 25     | 24     |
| PARITY              | OL_ILIMIT |        |             | OL_ACC_A1            |                       |        |        |
| R/W-0h              |           | R/W-0h |             |                      | R/W-0h                |        |        |
| 23                  | 22        | 21     | 20          | 19                   | 18                    | 17     | 16     |
| OL_ACC_A1           | OL_ACC_A2 |        |             | AUTO_HANDOFF_FF_EN   | OPN_CL_HANDOFF_THR    |        |        |
| R/W-0h              |           | R/W-0h |             |                      | R/W-0h                |        | R/W-0h |
| 15                  | 14        | 13     | 12          | 11                   | 10                    | 9      | 8      |
| OPN_CL_HANDOFF_THR  |           |        | ALIGN_ANGLE |                      |                       |        |        |
| R/W-0h              |           |        | R/W-0h      |                      |                       |        |        |
| 7                   | 6         | 5      | 4           | 3                    | 2                     | 1      | 0      |
| SLOW_FIRST_CYC_FREQ |           |        |             | FIRST_CYCLE_FREQ_SEL | THETA_ERROR_RAMP_RATE |        |        |
| R/W-0h              |           |        |             | R/W-0h               |                       | R/W-0h |        |

**表 7-18. MOTOR\_STARTUP2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 31    | PARITY    | R/W  | 0h    | Parity bit   |
| 30-27 | OL_ILIMIT | R/W  | 0h    | Open loop current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |

**表 7-18. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit   | Field           | Type | Reset | Description  |
|-------|-----------------|------|-------|--|
| 26-23 | OL_ACC_A1       | R/W  | 0h    | Open loop acceleration coefficient A1<br>0h = 0.01 Hz/s<br>1h = 0.05 Hz/s<br>2h = 1 Hz/s<br>3h = 2.5 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 25 Hz/s<br>7h = 50 Hz/s<br>8h = 75 Hz/s<br>9h = 100 Hz/s<br>Ah = 250 Hz/s<br>Bh = 500 Hz/s<br>Ch = 750 Hz/s<br>Dh = 1000 Hz/s<br>Eh = 5000 Hz/s<br>Fh = 10000 Hz/s  |
| 22-19 | OL_ACC_A2       | R/W  | 0h    | Open loop acceleration coefficient A2<br>0h = 0.0 Hz/s <sup>2</sup><br>1h = 0.05 Hz/s <sup>2</sup><br>2h = 1 Hz/s <sup>2</sup><br>3h = 2.5 Hz/s <sup>2</sup><br>4h = 5 Hz/s <sup>2</sup><br>5h = 10 Hz/s <sup>2</sup><br>6h = 25 Hz/s <sup>2</sup><br>7h = 50 Hz/s <sup>2</sup><br>8h = 75 Hz/s <sup>2</sup><br>9h = 100 Hz/s <sup>2</sup><br>Ah = 250 Hz/s <sup>2</sup><br>Bh = 500 Hz/s <sup>2</sup><br>Ch = 750 Hz/s <sup>2</sup><br>Dh = 1000 Hz/s <sup>2</sup><br>Eh = 5000 Hz/s <sup>2</sup><br>Fh = 10000 Hz/s <sup>2</sup> |
| 18    | AUTO_HANDOFF_EN | R/W  | 0h    | Auto handoff enable<br>0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR)<br>1h = Enable Auto Handoff  |

表 7-18. MOTOR\_STARTUP2 Register Field Descriptions (continued)

| Bit   | Field              | Type | Reset | Description  |
|-------|--------------------|------|-------|--|
| 17-13 | OPN_CL_HANDOFF_THR | R/W  | 0h    | Open to close loop handoff threshold (% of MAX_SPEED)<br>0h = 1%<br>1h = 2%<br>2h = 3%<br>3h = 4%<br>4h = 5%<br>5h = 6%<br>6h = 7%<br>7h = 8%<br>8h = 9%<br>9h = 10%<br>Ah = 11%<br>Bh = 12%<br>Ch = 13%<br>Dh = 14%<br>Eh = 15%<br>Fh = 16%<br>10h = 17%<br>11h = 18%<br>12h = 19%<br>13h = 20%<br>14h = 22.5%<br>15h = 25%<br>16h = 27.5%<br>17h = 30%<br>18h = 32.5%<br>19h = 35%<br>1Ah = 37.5%<br>1Bh = 40%<br>1Ch = 42.5%<br>1Dh = 45%<br>1Eh = 47.5%<br>1Fh = 50% |



**表 7-18. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description  |
|------|-------------------------|------|-------|--|
| 12-8 | ALIGN_ANGLE             | R/W  | 0h    | Align angle<br>0h = 0°<br>1h = 10°<br>2h = 20°<br>3h = 30°<br>4h = 45°<br>5h = 60°<br>6h = 70°<br>7h = 80°<br>8h = 90°<br>9h = 110°<br>Ah = 120°<br>Bh = 135°<br>Ch = 150°<br>Dh = 160°<br>Eh = 170°<br>Fh = 180°<br>10h = 190°<br>11h = 210°<br>12h = 225°<br>13h = 240°<br>14h = 250°<br>15h = 260°<br>16h = 270°<br>17h = 280°<br>18h = 290°<br>19h = 315°<br>1Ah = 330°<br>1Bh = 340°<br>1Ch = 350°<br>1Dh = N/A<br>1Eh = N/A<br>1Fh = N/A |
| 7-4  | SLOW_FIRST_CYC_FRE<br>Q | R/W  | 0h    | Frequency of first cycle in close loop startup (% of MAX_SPEED)<br>0h = 1%<br>1h = 2%<br>2h = 3%<br>3h = 5%<br>4h = 7.5%<br>5h = 10%<br>6h = 12.5%<br>7h = 15%<br>8h = 17.5%<br>9h = 20%<br>Ah = 25%<br>Bh = 30%<br>Ch = 35%<br>Dh = 40%<br>Eh = 45%<br>Fh = 50%   |

**表 7-18. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 3   | FIRST_CYCLE_FREQ_SEL  | R/W  | 0h    | First cycle frequency in open loop for align, double align and IPD startup options<br>0h = Defined by SLOW_FIRST_CYC_FREQ<br>1h = 0 Hz   |
| 2-0 | THETA_ERROR_RAMP_RATE | R/W  | 0h    | Ramp rate for reducing difference between estimated theta and open loop theta<br>0h = 0.01 deg/ms<br>1h = 0.05 deg/ms<br>2h = 0.1 deg/ms<br>3h = 0.15 deg/ms<br>4h = 0.2 deg/ms<br>5h = 0.5 deg/ms<br>6h = 1 deg/ms<br>7h = 2 deg/ms |

### 7.7.1.5 CLOSED\_LOOP1 Register (Address = 88h) [Reset = 0000000h]

CLOSED\_LOOP1 is shown in [CLOSED\\_LOOP1 Register](#) and described in [CLOSED\\_LOOP1 Register Field Descriptions](#).

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Register to configure close loop settings1

**图 7-59. CLOSED\_LOOP1 Register**

|                 |  |                       |  |        |  |              |  |                  |  |                |  |                           |  |    |  |
|-----------------|--|-----------------------|--|--------|--|--------------|--|------------------|--|----------------|--|---------------------------|--|----|--|
| 31              |  | 30                    |  | 29     |  | 28           |  | 27               |  | 26             |  | 25                        |  | 24 |  |
| PARITY          |  | OVERMODULATION_ENABLE |  | CL_ACC |  |              |  |                  |  | CL_DEC_CONFIG  |  |                           |  |    |  |
| R/W-0h          |  | R/W-0h                |  | R/W-0h |  |              |  |                  |  | R/W-0h         |  |                           |  |    |  |
| 23              |  | 22                    |  | 21     |  | 20           |  | 19               |  | 18             |  | 17                        |  | 16 |  |
| CL_DEC          |  |                       |  |        |  | PWM_FREQ_OUT |  |                  |  |                |  |                           |  |    |  |
| R/W-0h          |  |                       |  |        |  | R/W-0h       |  |                  |  |                |  |                           |  |    |  |
| 15              |  | 14                    |  | 13     |  | 12           |  | 11               |  | 10             |  | 9                         |  | 8  |  |
| PWM_FREQ_OUTPUT |  | PWM_MODE              |  | FG_SEL |  |              |  | FG_DIV           |  |                |  |                           |  |    |  |
| R/W-0h          |  | R/W-0h                |  | R/W-0h |  |              |  | R/W-0h           |  |                |  |                           |  |    |  |
| 7               |  | 6                     |  | 5      |  | 4            |  | 3                |  | 2              |  | 1                         |  | 0  |  |
| FG_CONFIG       |  | FG_BEMF_THR           |  |        |  | AVS_EN       |  | DEADTIME_COMP_EN |  | SPEED_LOOP_DIS |  | LOW_SPEED_RECIRC_BRAKE_EN |  |    |  |
| R/W-0h          |  | R/W-0h                |  |        |  | R/W-0h       |  | R/W-0h           |  | R/W-0h         |  | R/W-0h                    |  |    |  |

**表 7-19. CLOSED\_LOOP1 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 31  | PARITY                | R/W  | 0h    | Parity bit   |
| 30  | OVERMODULATION_ENABLE | R/W  | 0h    | Overmodulation enable<br>0h = Disable Over Modulation<br>1h = Enable Over Modulation |

表 7-19. CLOSED\_LOOP1 Register Field Descriptions (continued)

| Bit   | Field         | Type | Reset | Description  |
|-------|---------------|------|-------|--|
| 29-25 | CL_ACC        | R/W  | 0h    | Closed loop acceleration<br>0h = 0.5 Hz/s<br>1h = 1 Hz/s<br>2h = 2.5 Hz/s<br>3h = 5 Hz/s<br>4h = 7.5 Hz/s<br>5h = 10 Hz/s<br>6h = 20 Hz/s<br>7h = 40 Hz/s<br>8h = 60 Hz/s<br>9h = 80 Hz/s<br>Ah = 100 Hz/s<br>Bh = 200 Hz/s<br>Ch = 300 Hz/s<br>Dh = 400 Hz/s<br>Eh = 500 Hz/s<br>Fh = 600 Hz/s<br>10h = 700 Hz/s<br>11h = 800 Hz/s<br>12h = 900 Hz/s<br>13h = 1000 Hz/s<br>14h = 2000 Hz/s<br>15h = 4000 Hz/s<br>16h = 6000 Hz/s<br>17h = 8000 Hz/s<br>18h = 10000 Hz/s<br>19h = 20000 Hz/s<br>1Ah = 30000 Hz/s<br>1Bh = 40000 Hz/s<br>1Ch = 50000 Hz/s<br>1Dh = 60000 Hz/s<br>1Eh = 70000 Hz/s<br>1Fh = No limit |
| 24    | CL_DEC_CONFIG | R/W  | 0h    | Closed loop deceleration configuration<br>0h = Closed loop deceleration defined by CL_DEC<br>1h = Closed loop deceleration defined by CL_ACC   |

**表 7-19. CLOSED\_LOOP1 Register Field Descriptions (continued)**

| Bit   | Field        | Type | Reset | Description  |
|-------|--------------|------|-------|--|
| 23-19 | CL_DEC       | R/W  | 0h    | <p>Closed loop deceleration. This register is used only if AVS is disabled and CL_DEC_CONFIG is set to '0'</p> <p>0h = 0.5 Hz/s<br/>           1h = 1 Hz/s<br/>           2h = 2.5 Hz/s<br/>           3h = 5 Hz/s<br/>           4h = 7.5 Hz/s<br/>           5h = 10 Hz/s<br/>           6h = 20 Hz/s<br/>           7h = 40 Hz/s<br/>           8h = 60 Hz/s<br/>           9h = 80 Hz/s<br/>           Ah = 100 Hz/s<br/>           Bh = 200 Hz/s<br/>           Ch = 300 Hz/s<br/>           Dh = 400 Hz/s<br/>           Eh = 500 Hz/s<br/>           Fh = 600 Hz/s<br/>           10h = 700 Hz/s<br/>           11h = 800 Hz/s<br/>           12h = 900 Hz/s<br/>           13h = 1000 Hz/s<br/>           14h = 2000 Hz/s<br/>           15h = 4000 Hz/s<br/>           16h = 6000 Hz/s<br/>           17h = 8000 Hz/s<br/>           18h = 10000 Hz/s<br/>           19h = 20000 Hz/s<br/>           1Ah = 30000 Hz/s<br/>           1Bh = 40000 Hz/s<br/>           1Ch = 50000 Hz/s<br/>           1Dh = 60000 Hz/s<br/>           1Eh = 70000 Hz/s<br/>           1Fh = No limit</p> |
| 18-15 | PWM_FREQ_OUT | R/W  | 0h    | <p>Output PWM switching frequency</p> <p>0h = 10 kHz<br/>           1h = 15 kHz<br/>           2h = 20 kHz<br/>           3h = 25 kHz<br/>           4h = 30 kHz<br/>           5h = 35 kHz<br/>           6h = 40 kHz<br/>           7h = 45 kHz<br/>           8h = 50 kHz<br/>           9h = 55 kHz<br/>           Ah = 60 kHz<br/>           Bh = 65 kHz<br/>           Ch = 70 kHz<br/>           Dh = 75 kHz<br/>           Eh = N/A<br/>           Fh = N/A</p>  |

表 7-19. CLOSED\_LOOP1 Register Field Descriptions (continued)

| Bit   | Field                         | Type | Reset | Description  |
|-------|-------------------------------|------|-------|--|
| 14    | PWM_MODE                      | R/W  | 0h    | PWM modulation<br>0h = Continuous Space Vector Modulation<br>1h = Discontinuous Space Vector Modulation  |
| 13-12 | FG_SEL                        | R/W  | 0h    | FG select<br>0h = Output FG in open loop and closed loop<br>1h = Output FG in only closed loop<br>2h = Output FG in open loop for the first try.<br>3h = N/A   |
| 11-8  | FG_DIV                        | R/W  | 0h    | FG division factor<br>0h = Divide by 1 (2-pole motor mechanical speed)<br>1h = Divide by 1 (2-pole motor mechanical speed)<br>2h = Divide by 2 (4-pole motor mechanical speed)<br>3h = Divide by 3 (6-pole motor mechanical speed)<br>4h = Divide by 4 (8-pole motor mechanical speed) ...<br>Fh = Divide by 15 (30-pole motor mechanical speed) |
| 7     | FG_CONFIG                     | R/W  | 0h    | FG output configuration<br>0h = FG active as long as motor is driven<br>1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR   |
| 6-4   | FG_BEMF_THR                   | R/W  | 0h    | FG output BEMF threshold<br>0h = +/- 1mV<br>1h = +/- 2mV<br>2h = +/- 5mV<br>3h = +/- 10mV<br>4h = +/- 20mV<br>5h = +/- 30mV<br>6h = N/A<br>7h = N/A  |
| 3     | AVS_EN                        | R/W  | 0h    | AVS enable<br>0h = Disable<br>1h = Enable  |
| 2     | DEADTIME_COMP_EN              | R/W  | 0h    | Deadtime compensation enable<br>0h = Disable<br>1h = Enable  |
| 1     | SPEED_LOOP_DIS                | R/W  | 0h    | Speed loop disable<br>0h = Enable<br>1h = Disable  |
| 0     | LOW_SPEED_RECIRC_B<br>RAKE_EN | R/W  | 0h    | Stop mode applied when stop mode is recirculation brake and motor running in align or open loop<br>0h = Hi-z<br>1h = Low Side Brake  |

### 7.7.1.6 CLOSED\_LOOP2 Register (Address = 8Ah) [Reset = 0000000h]

CLOSED\_LOOP2 is shown in [CLOSED\\_LOOP2 Register](#) and described in [CLOSED\\_LOOP2 Register Field Descriptions](#).

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Register to configure close loop settings2

**图 7-60. CLOSED\_LOOP2 Register**

|              |    |          |    |                       |                   |    |    |
|--------------|----|----------|----|-----------------------|-------------------|----|----|
| 31           | 30 | 29       | 28 | 27                    | 26                | 25 | 24 |
| PARITY       |    | MTR_STOP |    |                       | MTR_STOP_BRK_TIME |    |    |
| R/W-0h       |    | R/W-0h   |    |                       | R/W-0h            |    |    |
| 23           | 22 | 21       | 20 | 19                    | 18                | 17 | 16 |
| ACT_SPIN_THR |    |          |    | BRAKE_SPEED_THRESHOLD |                   |    |    |
| R/W-0h       |    |          |    | R/W-0h                |                   |    |    |
| 15           | 14 | 13       | 12 | 11                    | 10                | 9  | 8  |
| MOTOR_RES    |    |          |    |                       |                   |    |    |
| R/W-0h       |    |          |    |                       |                   |    |    |
| 7            | 6  | 5        | 4  | 3                     | 2                 | 1  | 0  |
| MOTOR_IND    |    |          |    |                       |                   |    |    |
| R/W-0h       |    |          |    |                       |                   |    |    |

**表 7-20. CLOSED\_LOOP2 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description  |
|-------|-------------------|------|-------|--|
| 31    | PARITY            | R/W  | 0h    | Parity bit   |
| 30-28 | MTR_STOP          | R/W  | 0h    | Motor stop method<br>0h = Hi-z<br>1h = Recirculation Mode<br>2h = Low side braking<br>3h = High side braking<br>4h = Active spin down<br>5h = Align braking<br>6h = N/A<br>7h = N/A  |
| 27-24 | MTR_STOP_BRK_TIME | R/W  | 0h    | Brake time during motor stop<br>0h = 0.1 ms<br>1h = 0.1 ms<br>2h = 0.25 ms<br>3h = 0.5 ms<br>4h = 1 ms<br>5h = 5 ms<br>6h = 10 ms<br>7h = 50 ms<br>8h = 100 ms<br>9h = 250 ms<br>Ah = 500 ms<br>Bh = 1000 ms<br>Ch = 2500 ms<br>Dh = 5000 ms<br>Eh = 10000 ms<br>Fh = 15000 ms |

表 7-20. CLOSED\_LOOP2 Register Field Descriptions (continued)

| Bit   | Field                     | Type | Reset | Description  |
|-------|---------------------------|------|-------|--|
| 23-20 | ACT_SPIN_THR              | R/W  | 0h    | Speed threshold for active spin down (% of MAX_SPEED)<br>0h = 100 %<br>1h = 90 %<br>2h = 80 %<br>3h = 70 %<br>4h = 60%<br>5h = 50 %<br>6h = 45 %<br>7h = 40 %<br>8h = 35 %<br>9h = 30 %<br>Ah = 25 %<br>Bh = 20 %<br>Ch = 15 %<br>Dh = 10 %<br>Eh = 5 %<br>Fh = 2.5 %  |
| 19-16 | BRAKE_SPEED_THRES<br>HOLD | R/W  | 0h    | Speed threshold for BRAKE pin and motor stop options (low-side braking or high-side braking or align braking) (% of MAX_SPEED)<br>0h = 100 %<br>1h = 90 %<br>2h = 80 %<br>3h = 70 %<br>4h = 60%<br>5h = 50 %<br>6h = 45 %<br>7h = 40 %<br>8h = 35 %<br>9h = 30 %<br>Ah = 25 %<br>Bh = 20 %<br>Ch = 15 %<br>Dh = 10 %<br>Eh = 5 %<br>Fh = 2.5 % |
| 15-8  | MOTOR_RES                 | R/W  | 0h    | 8-bit values for motor phase resistance  |
| 7-0   | MOTOR_IND                 | R/W  | 0h    | 8-bit values for motor phase inductance  |



### 7.7.1.7 CLOSED\_LOOP3 Register (Address = 8Ch) [Reset = 0000000h]

CLOSED\_LOOP3 is shown in [CLOSED\\_LOOP3 Register](#) and described in [CLOSED\\_LOOP3 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure close loop settings3

**图 7-61. CLOSED\_LOOP3 Register**

|                  |    |                  |    |              |             |    |    |
|------------------|----|------------------|----|--------------|-------------|----|----|
| 31               | 30 | 29               | 28 | 27           | 26          | 25 | 24 |
| PARITY           |    | MOTOR_BEMF_CONST |    |              |             |    |    |
| R/W-0h           |    | R/W-0h           |    |              |             |    |    |
| 23               | 22 | 21               | 20 | 19           | 18          | 17 | 16 |
| MOTOR_BEMF_CONST |    | CURR_LOOP_KP     |    |              |             |    |    |
| R/W-0h           |    | R/W-0h           |    |              |             |    |    |
| 15               | 14 | 13               | 12 | 11           | 10          | 9  | 8  |
| CURR_LOOP_KP     |    |                  |    | CURR_LOOP_KI |             |    |    |
| R/W-0h           |    |                  |    | R/W-0h       |             |    |    |
| 7                | 6  | 5                | 4  | 3            | 2           | 1  | 0  |
| CURR_LOOP_KI     |    |                  |    |              | SPD_LOOP_KP |    |    |
| R/W-0h           |    |                  |    |              | R/W-0h      |    |    |

**表 7-21. CLOSED\_LOOP3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 31    | PARITY           | R/W  | 0h    | Parity bit  |
| 30-23 | MOTOR_BEMF_CONST | R/W  | 0h    | 8-bit values for motor BEMF constant  |
| 22-13 | CURR_LOOP_KP     | R/W  | 0h    | 10-bit value for current Iq and Id loop Kp. $K_p = 8\text{LSB of CURR\_LOOP\_KP} / 10^2\text{MSB of CURR\_LOOP\_KP}$ . Set to 0 for auto calculation of current loop Kp.        |
| 12-3  | CURR_LOOP_KI     | R/W  | 0h    | 10-bit value for current Iq and Id loop Ki. $K_i = 1000 * 8\text{LSB of CURR\_LOOP\_KI} / 10^2\text{MSB of CURR\_LOOP\_KI}$ . Set to 0 for auto calculation of current loop Ki. |
| 2-0   | SPD_LOOP_KP      | R/W  | 0h    | 3 MSB bits for speed loop Kp. $K_p = 0.01 * 8\text{LSB of SPD\_LOOP\_KP} / 10^2\text{MSB of SPD\_LOOP\_KP}$   |

### 7.7.1.8 CLOSED\_LOOP4 Register (Address = 8Eh) [Reset = X]

CLOSED\_LOOP4 is shown in [CLOSED\\_LOOP4 Register](#) and described in [CLOSED\\_LOOP4 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure close loop settings4

**图 7-62. CLOSED\_LOOP4 Register**

|             |    |             |    |    |    |    |    |
|-------------|----|-------------|----|----|----|----|----|
| 31          | 30 | 29          | 28 | 27 | 26 | 25 | 24 |
| PARITY      |    | SPD_LOOP_KP |    |    |    |    |    |
| R/W-0h      |    | R/W-0h      |    |    |    |    |    |
| 23          | 22 | 21          | 20 | 19 | 18 | 17 | 16 |
| SPD_LOOP_KI |    |             |    |    |    |    |    |
| R/W-0h      |    |             |    |    |    |    |    |
| 15          | 14 | 13          | 12 | 11 | 10 | 9  | 8  |
| SPD_LOOP_KI |    | MAX_SPEED   |    |    |    |    |    |
| R/W-0h      |    | R/W-X       |    |    |    |    |    |
| 7           | 6  | 5           | 4  | 3  | 2  | 1  | 0  |
| MAX_SPEED   |    |             |    |    |    |    |    |
| R/W-X       |    |             |    |    |    |    |    |

**表 7-22. CLOSED\_LOOP4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description  |
|-------|-------------|------|-------|--|
| 31    | PARITY      | R/W  | 0h    | Parity bit   |
| 30-24 | SPD_LOOP_KP | R/W  | 0h    | 7 LSB bits for speed loop Kp. $K_p = 0.01 * 8\text{LSB of SPD\_LOOP\_KP} / 10^2\text{MSB of SPD\_LOOP\_KP}$ . Set to 0 for auto calculation of speed loop Kp.  |
| 23-14 | SPD_LOOP_KI | R/W  | 0h    | 10-bit value for speed loop Ki. $K_i = 0.1 * 8\text{LSB of SPD\_LOOP\_KI} / 10^2\text{MSB of SPD\_LOOP\_KI}$ . Set to 0 for auto calculation of speed loop Ki.   |
| 13-0  | MAX_SPEED   | R/W  | X     | 14-bit value for setting maximum value of speed in electrical Hz<br>Maximum motor electrical speed (Hz): $\{\text{MOTOR\_SPEED}/6\}$<br>For example: if MOTOR_SPEED is 0x2710, then maximum motor speed (Hz) = $10000(0x2710)/6 = 1666$ Hz |

### 7.7.1.9 SPEED\_PROFILES1 Register (Address = 94h) [Reset = X]

SPEED\_PROFILES1 is shown in [SPEED\\_PROFILES1 Register](#) and described in [SPEED\\_PROFILES1 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile1

**图 7-63. SPEED\_PROFILES1 Register**

|             |                      |    |             |          |    |    |    |
|-------------|----------------------|----|-------------|----------|----|----|----|
| 31          | 30                   | 29 | 28          | 27       | 26 | 25 | 24 |
| PARITY      | SPEED_PROFILE_CONFIG |    |             | DUTY_ON1 |    |    |    |
| R/W-0h      | R/W-0h               |    |             | R/W-X    |    |    |    |
| 23          | 22                   | 21 | 20          | 19       | 18 | 17 | 16 |
| DUTY_ON1    |                      |    | DUTY_OFF1   |          |    |    |    |
| R/W-X       |                      |    | R/W-X       |          |    |    |    |
| 15          | 14                   | 13 | 12          | 11       | 10 | 9  | 8  |
| DUTY_OFF1   |                      |    | DUTY_CLAMP1 |          |    |    |    |
| R/W-X       |                      |    | R/W-X       |          |    |    |    |
| 7           | 6                    | 5  | 4           | 3        | 2  | 1  | 0  |
| DUTY_CLAMP1 |                      |    | DUTY_A      |          |    |    |    |
| R/W-X       |                      |    | R/W-X       |          |    |    |    |

**表 7-23. SPEED\_PROFILES1 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 31    | PARITY               | R/W  | 0h    | Parity bit  |
| 30-29 | SPEED_PROFILE_CONFIG | R/W  | 0h    | Configuration for speed profiles<br>0h = Speed Reference Mode<br>1h = Linear Mode<br>2h = Staircase Mode<br>3h = Forward Reverse Mode |
| 28-21 | DUTY_ON1             | R/W  | X     | Duty_ON1 configuration (%) = $\{(DUTY\_ON1/255)*100\}$  |
| 20-13 | DUTY_OFF1            | R/W  | X     | Duty_OFF1 Configuration (%) = $\{(DUTY\_OFF1/255)*100\}$  |
| 12-5  | DUTY_CLAMP1          | R/W  | X     | Duty_CLAMP1 Configuration Duty Cycle for clamping speed (%) = $\{(DUTY\_CLAMP1/255)*100\}$  |
| 4-0   | DUTY_A               | R/W  | X     | 5 MSB bits for Duty Cycle A   |

### 7.7.1.10 SPEED\_PROFILES2 Register (Address = 96h) [Reset = X]

SPEED\_PROFILES2 is shown in [SPEED\\_PROFILES2 Register](#) and described in [SPEED\\_PROFILES2 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile2

**图 7-64. SPEED\_PROFILES2 Register**

|        |        |    |        |        |    |    |    |
|--------|--------|----|--------|--------|----|----|----|
| 31     | 30     | 29 | 28     | 27     | 26 | 25 | 24 |
| PARITY | DUTY_A |    |        | DUTY_B |    |    |    |
| R/W-0h | R/W-X  |    |        | R/W-X  |    |    |    |
| 23     | 22     | 21 | 20     | 19     | 18 | 17 | 16 |
| DUTY_B |        |    | DUTY_C |        |    |    |    |
| R/W-X  |        |    | R/W-X  |        |    |    |    |
| 15     | 14     | 13 | 12     | 11     | 10 | 9  | 8  |
| DUTY_C |        |    | DUTY_D |        |    |    |    |
| R/W-X  |        |    | R/W-X  |        |    |    |    |
| 7      | 6      | 5  | 4      | 3      | 2  | 1  | 0  |
| DUTY_D |        |    | DUTY_E |        |    |    |    |
| R/W-X  |        |    | R/W-0h |        |    |    |    |

**表 7-24. SPEED\_PROFILES2 Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description   |
|-------|--------|------|-------|---|
| 31    | PARITY | R/W  | 0h    | Parity bit  |
| 30-28 | DUTY_A | R/W  | X     | 3 LSB bits for Duty Cycle A Duty_A Configuration Duty Cycle A (%) = $\{(DUTY\_A/255)*100\}$ |
| 27-20 | DUTY_B | R/W  | X     | Duty_B Configuration Duty Cycle B (%) = $\{(DUTY\_B/255)*100\}$                             |
| 19-12 | DUTY_C | R/W  | X     | Duty_C Configuration Duty Cycle C (%) = $\{(DUTY\_C/255)*100\}$                             |
| 11-4  | DUTY_D | R/W  | X     | Duty_D Configuration Duty Cycle D (%) = $\{(DUTY\_D/255)*100\}$                             |
| 3-0   | DUTY_E | R/W  | 0h    | 4 MSB bits for Duty Cycle E   |

### 7.7.1.11 SPEED\_PROFILES3 Register (Address = 98h) [Reset = X]

SPEED\_PROFILES3 is shown in [SPEED\\_PROFILES3 Register](#) and described in [SPEED\\_PROFILES3 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile3

**图 7-65. SPEED\_PROFILES3 Register**

|             |    |        |    |             |          |          |    |
|-------------|----|--------|----|-------------|----------|----------|----|
| 31          | 30 | 29     | 28 | 27          | 26       | 25       | 24 |
| PARITY      |    | DUTY_E |    |             |          | DUTY_ON2 |    |
| R/W-0h      |    | R/W-X  |    |             |          | R/W-X    |    |
| 23          | 22 | 21     | 20 | 19          | 18       | 17       | 16 |
| DUTY_ON2    |    |        |    | DUTY_OFF2   |          |          |    |
| R/W-X       |    |        |    | R/W-X       |          |          |    |
| 15          | 14 | 13     | 12 | 11          | 10       | 9        | 8  |
| DUTY_OFF2   |    |        |    | DUTY_CLAMP2 |          |          |    |
| R/W-X       |    |        |    | R/W-X       |          |          |    |
| 7           | 6  | 5      | 4  | 3           | 2        | 1        | 0  |
| DUTY_CLAMP2 |    |        |    |             | RESERVED |          |    |
| R/W-X       |    |        |    |             | R/W-0h   |          |    |

**表 7-25. SPEED\_PROFILES3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description   |
|-------|-------------|------|-------|---|
| 31    | PARITY      | R/W  | 0h    | Parity bit  |
| 30-27 | DUTY_E      | R/W  | X     | 4 LSB bits for Duty Cycle E Duty_E Configuration Duty Cycle E (%) = $\{(DUTY\_E/255)*100\}$ |
| 26-19 | DUTY_ON2    | R/W  | X     | Duty_ON2 Configuration (%) = $\{(DUTY\_ON2/255)*100\}$                                      |
| 18-11 | DUTY_OFF2   | R/W  | X     | Duty_OFF2 Configuration (%) = $\{(DUTY\_OFF2/255)*100\}$                                    |
| 10-3  | DUTY_CLAMP2 | R/W  | X     | Duty_CLAMP2 Configuration Duty Cycle for clamping speed (%) = $\{(DUTY\_CLAMP1/255)*100\}$  |
| 2-0   | RESERVED    | R/W  | 0h    | Reserved  |

**7.7.1.12 SPEED\_PROFILES4 Register (Address = 9Ah) [Reset = X]**

SPEED\_PROFILES4 is shown in [SPEED\\_PROFILES4 Register](#) and described in [SPEED\\_PROFILES4 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile4

**图 7-66. SPEED\_PROFILES4 Register**

|              |    |              |    |    |    |    |    |
|--------------|----|--------------|----|----|----|----|----|
| 31           | 30 | 29           | 28 | 27 | 26 | 25 | 24 |
| PARITY       |    | SPEED_OFF1   |    |    |    |    |    |
| R/W-0h       |    | R/W-X        |    |    |    |    |    |
| 23           | 22 | 21           | 20 | 19 | 18 | 17 | 16 |
| SPEED_OFF1   |    | SPEED_CLAMP1 |    |    |    |    |    |
| R/W-X        |    | R/W-X        |    |    |    |    |    |
| 15           | 14 | 13           | 12 | 11 | 10 | 9  | 8  |
| SPEED_CLAMP1 |    | SPEED_A      |    |    |    |    |    |
| R/W-X        |    | R/W-X        |    |    |    |    |    |
| 7            | 6  | 5            | 4  | 3  | 2  | 1  | 0  |
| SPEED_A      |    | SPEED_B      |    |    |    |    |    |
| R/W-X        |    | R/W-X        |    |    |    |    |    |

**表 7-26. SPEED\_PROFILES4 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description  |
|-------|--------------|------|-------|--|
| 31    | PARITY       | R/W  | 0h    | Parity bit   |
| 30-23 | SPEED_OFF1   | R/W  | X     | Turn off speed Configuration Turn off speed (% of MAX_SPEED) = $\{(SPEED\_OFF1/255)*100\}$ |
| 22-15 | SPEED_CLAMP1 | R/W  | X     | Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = $\{(SPEED\_CLAMP1/255)*100\}$     |
| 14-7  | SPEED_A      | R/W  | X     | Speed A configuration SPEED A (% of MAX_SPEED) = $\{(SPEED\_A/255)*100\}$                  |
| 6-0   | SPEED_B      | R/W  | X     | 7 MSB of SPEED_B configuration   |

### 7.7.1.13 SPEED\_PROFILES5 Register (Address = 9Ch) [Reset = X]

SPEED\_PROFILES5 is shown in [SPEED\\_PROFILES5 Register](#) and described in [SPEED\\_PROFILES5 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile5

**图 7-67. SPEED\_PROFILES5 Register**

|         |  |         |  |    |  |    |  |    |  |          |  |    |  |    |  |
|---------|--|---------|--|----|--|----|--|----|--|----------|--|----|--|----|--|
| 31      |  | 30      |  | 29 |  | 28 |  | 27 |  | 26       |  | 25 |  | 24 |  |
| PARITY  |  | SPEED_B |  |    |  |    |  |    |  | SPEED_C  |  |    |  |    |  |
| R/W-0h  |  | R/W-X   |  |    |  |    |  |    |  | R/W-X    |  |    |  |    |  |
| 23      |  | 22      |  | 21 |  | 20 |  | 19 |  | 18       |  | 17 |  | 16 |  |
| SPEED_C |  |         |  |    |  |    |  |    |  | SPEED_D  |  |    |  |    |  |
| R/W-X   |  |         |  |    |  |    |  |    |  | R/W-X    |  |    |  |    |  |
| 15      |  | 14      |  | 13 |  | 12 |  | 11 |  | 10       |  | 9  |  | 8  |  |
| SPEED_D |  |         |  |    |  |    |  |    |  | SPEED_E  |  |    |  |    |  |
| R/W-X   |  |         |  |    |  |    |  |    |  | R/W-X    |  |    |  |    |  |
| 7       |  | 6       |  | 5  |  | 4  |  | 3  |  | 2        |  | 1  |  | 0  |  |
| SPEED_E |  |         |  |    |  |    |  |    |  | RESERVED |  |    |  |    |  |
| R/W-X   |  |         |  |    |  |    |  |    |  | R/W-0h   |  |    |  |    |  |

**表 7-27. SPEED\_PROFILES5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 31    | PARITY   | R/W  | 0h    | Parity bit  |
| 30    | SPEED_B  | R/W  | X     | 1 LSB of SPEED_B configuration Speed B Configuration $SPEED\ B(\% \text{ of } MAX\_SPEED) = \{(SPEED\_B/255)*100\}$ |
| 29-22 | SPEED_C  | R/W  | X     | Speed C configuration SPEED C (% of MAX_SPEED) = $\{(SPEED\_A/255)*100\}$   |
| 21-14 | SPEED_D  | R/W  | X     | Speed D configuration SPEED D (% of MAX_SPEED) = $\{(SPEED\_D/255)*100\}$   |
| 13-6  | SPEED_E  | R/W  | X     | Speed E Configuration SPEED E (% of MAX_SPEED) = $\{(SPEED\_E/255)*100\}$   |
| 5-0   | RESERVED | R/W  | 0h    | Reserved  |

### 7.7.1.14 SPEED\_PROFILES6 Register (Address = 9Eh) [Reset = X]

SPEED\_PROFILES6 is shown in [SPEED\\_PROFILES6 Register](#) and described in [SPEED\\_PROFILES6 Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure speed profile6

**图 7-68. SPEED\_PROFILES6 Register**

|              |              |    |    |    |    |    |    |
|--------------|--------------|----|----|----|----|----|----|
| 31           | 30           | 29 | 28 | 27 | 26 | 25 | 24 |
| PARITY       | SPEED_OFF2   |    |    |    |    |    |    |
| R/W-0h       | R/W-X        |    |    |    |    |    |    |
| 23           | 22           | 21 | 20 | 19 | 18 | 17 | 16 |
| SPEED_OFF2   | SPEED_CLAMP2 |    |    |    |    |    |    |
| R/W-X        | R/W-X        |    |    |    |    |    |    |
| 15           | 14           | 13 | 12 | 11 | 10 | 9  | 8  |
| SPEED_CLAMP2 | RESERVED     |    |    |    |    |    |    |
| R/W-X        | R/W-X        |    |    |    |    |    |    |
| 7            | 6            | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED     |              |    |    |    |    |    |    |
| R/W-X        |              |    |    |    |    |    |    |

**表 7-28. SPEED\_PROFILES6 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description  |
|-------|--------------|------|-------|--|
| 31    | PARITY       | R/W  | 0h    | Parity bit   |
| 30-23 | SPEED_OFF2   | R/W  | X     | Turn off speed Configuration Turn off speed (% of MAX_SPEED) = $\{(SPEED\_OFF2/255)*100\}$ |
| 22-15 | SPEED_CLAMP2 | R/W  | X     | Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = $\{(SPEED\_CLAMP2/255)*100\}$     |
| 14-0  | RESERVED     | R/W  | X     | Reserved   |

### 7.7.2 Fault\_Configuration Registers

[FAULT\\_CONFIGURATION Registers](#) lists the memory-mapped registers for the Fault\_Configuration registers. All register offset addresses not listed in [FAULT\\_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

**表 7-29. FAULT\_CONFIGURATION Registers**

| Address | Acronym       | Register Name         | Section                   |
|---------|---------------|-----------------------|---------------------------|
| 90h     | FAULT_CONFIG1 | Fault Configuration 1 | <a href="#">节 7.7.2.1</a> |
| 92h     | FAULT_CONFIG2 | Fault Configuration 2 | <a href="#">节 7.7.2.2</a> |

Complex bit access types are encoded to fit into small table cells. [Fault\\_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

**表 7-30. Fault\_Configuration Access Type Codes**

| Access Type       | Code | Description |
|-------------------|------|-------------|
| <b>Read Type</b>  |      |             |
| R                 | R    | Read        |
| <b>Write Type</b> |      |             |
| W                 | W    | Write       |



**表 7-30. Fault\_Configuration Access Type Codes  
(continued)**

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Reset or Default Value</b> |      |  |
| <i>-n</i>                     |      | Value after reset or the default value |

**7.7.2.1 FAULT\_CONFIG1 Register (Address = 90h) [Reset = 0000000h]**

FAULT\_CONFIG1 is shown in [FAULT\\_CONFIG1 Register](#) and described in [FAULT\\_CONFIG1 Register Field Descriptions](#).

Return to the [FAULT\\_CONFIGURATION Registers](#).

Register to configure fault settings1

**图 7-69. FAULT\_CONFIG1 Register**

|                  |                 |        |    |                      |                   |                     |        |
|------------------|-----------------|--------|----|----------------------|-------------------|---------------------|--------|
| 31               | 30              | 29     | 28 | 27                   | 26                | 25                  | 24     |
| PARITY           | ILIMIT          |        |    | HW_LOCK_ILIMIT       |                   |                     |        |
| R/W-0h           |                 | R/W-0h |    |                      | R/W-0h            |                     |        |
| 23               | 22              | 21     | 20 | 19                   | 18                | 17                  | 16     |
| HW_LOCK_ILIMIT   | LOCK_ILIMIT     |        |    | LOCK_ILIMIT_MODE     |                   |                     |        |
| R/W-0h           |                 | R/W-0h |    |                      | R/W-0h            |                     |        |
| 15               | 14              | 13     | 12 | 11                   | 10                | 9                   | 8      |
| LOCK_ILIMIT_MODE | LOCK_ILIMIT_DEG |        |    | LCK_RETRY            |                   |                     |        |
| R/W-0h           |                 | R/W-0h |    |                      | R/W-0h            |                     |        |
| 7                | 6               | 5      | 4  | 3                    | 2                 | 1                   | 0      |
| LCK_RETRY        | MTR_LCK_MODE    |        |    | IPD_TIMEOUT_FAULT_EN | IPD_FREQ_FAULT_EN | SATURATION_FLAGS_EN |        |
| R/W-0h           |                 | R/W-0h |    |                      | R/W-0h            | R/W-0h              | R/W-0h |

**表 7-31. FAULT\_CONFIG1 Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description   |
|-------|--------|------|-------|---|
| 31    | PARITY | R/W  | 0h    | Parity bit  |
| 30-27 | ILIMIT | R/W  | 0h    | Reference for torque PI loop<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |

**表 7-31. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 26-23 | HW_LOCK_ILIMIT | R/W  | 0h    | Comparator based lock detection current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |
| 22-19 | LOCK_ILIMIT    | R/W  | 0h    | ADC based lock detection current threshold<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A    |

表 7-31. FAULT\_CONFIG1 Register Field Descriptions (continued)

| Bit   | Field            | Type | Reset | Description  |
|-------|------------------|------|-------|--|
| 18-15 | LOCK_ILIMIT_MODE | R/W  | 0h    | <p>Lock current limit mode</p> <p>0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated</p> <p>1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode</p> <p>2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON)</p> <p>3h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFAULT active</p> <p>6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high-side brake mode (All-high side FETs are turned ON); nFAULT active</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low-side brake mode (All-low side FETs are turned ON); nFAULT active</p> <p>8h = Ilimit lock detection current limit is in report only but no action is taken; nFAULT active</p> <p>9h = ILIMIT LOCK is disabled</p> <p>Ah = ILIMIT LOCK is disabled</p> <p>Bh = ILIMIT LOCK is disabled</p> <p>Ch = ILIMIT LOCK is disabled</p> <p>Dh = ILIMIT LOCK is disabled</p> <p>Eh = ILIMIT LOCK is disabled</p> <p>Fh = ILIMIT LOCK is disabled</p> |
| 14-11 | LOCK_ILIMIT_DEG  | R/W  | 0h    | <p>Lock detection current limit deglitch time</p> <p>0h = 0.05 ms</p> <p>1h = 0.1 ms</p> <p>2h = 0.2 ms</p> <p>3h = 0.5 ms</p> <p>4h = 1 ms</p> <p>5h = 2.5 ms</p> <p>6h = 5 ms</p> <p>7h = 7.5 ms</p> <p>8h = 10 ms</p> <p>9h = 25 ms</p> <p>Ah = 50 ms</p> <p>Bh = 75 ms</p> <p>Ch = 100 ms</p> <p>Dh = 200 ms</p> <p>Eh = 500 ms</p> <p>Fh = 1000 ms</p>  |

**表 7-31. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--|
| 10-7 | LCK_RETRY    | R/W  | 0h    | <p>Lock detection retry time</p> <p>0h = 100 ms</p> <p>1h = 500 ms</p> <p>2h = 1 s</p> <p>3h = 2 s</p> <p>4h = 3 s</p> <p>5h = 4 s</p> <p>6h = 5 s</p> <p>7h = 6 s</p> <p>8h = 7 s</p> <p>9h = 8 s</p> <p>Ah = 9 s</p> <p>Bh = 10 s</p> <p>Ch = 11 s</p> <p>Dh = 12 s</p> <p>Eh = 13 s</p> <p>Fh = 14 s</p>  |
| 6-3  | MTR_LCK_MODE | R/W  | 0h    | <p>Motor Lock Mode</p> <p>0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated</p> <p>1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode</p> <p>2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON)</p> <p>3h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFAULT active</p> <p>6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high-side brake mode (All high-side FETs are turned ON); nFAULT active</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low-side brake mode (All low-side FETs are turned ON); nFAULT active</p> <p>8h = Motor lock detection current limit is in report only but no action is taken; nFAULT active</p> <p>9h = Motor lock detection is disabled</p> <p>Ah = Motor lock detection is disabled</p> <p>Bh = Motor lock detection is disabled</p> <p>Ch = Motor lock detection is disabled</p> <p>Dh = Motor lock detection is disabled</p> <p>Eh = Motor lock detection is disabled</p> <p>Fh = Motor lock detection is disabled</p> |

**表 7-31. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit | Field                     | Type | Reset | Description   |
|-----|---------------------------|------|-------|---|
| 2   | IPD_TIMEOUT_FAULT_EN<br>N | R/W  | 0h    | IPD timeout fault enable<br>0h = Disable<br>1h = Enable                                     |
| 1   | IPD_FREQ_FAULT_EN         | R/W  | 0h    | IPD frequency fault enable<br>0h = Disable<br>1h = Enable                                   |
| 0   | SATURATION_FLAGS_EN<br>N  | R/W  | 0h    | Enables indication of current loop and speed loop saturation<br>0h = Disable<br>1h = Enable |

### 7.7.2.2 FAULT\_CONFIG2 Register (Address = 92h) [Reset = 0000000h]

FAULT\_CONFIG2 is shown in [FAULT\\_CONFIG2 Register](#) and described in [FAULT\\_CONFIG2 Register Field Descriptions](#).

Return to the [FAULT\\_CONFIGURATION Registers](#).

Register to configure fault settings2

图 7-70. FAULT\_CONFIG2 Register

|                     |                    |            |          |                |                     |                   |    |
|---------------------|--------------------|------------|----------|----------------|---------------------|-------------------|----|
| 31                  | 30                 | 29         | 28       | 27             | 26                  | 25                | 24 |
| PARITY              | LOCK1_EN           | LOCK2_EN   | LOCK3_EN | LOCK_ABN_SPEED |                     | ABNORMAL_BEMF_THR |    |
| R/W-0h              | R/W-0h             | R/W-0h     | R/W-0h   | R/W-0h         |                     | R/W-0h            |    |
| 23                  | 22                 | 21         | 20       | 19             | 18                  | 17                | 16 |
| ABNORMAL_BEMF_THR   |                    | NO_MTR_THR |          |                | HW_LOCK_ILIMIT_MODE |                   |    |
| R/W-0h              |                    | R/W-0h     |          |                | R/W-0h              |                   |    |
| 15                  | 14                 | 13         | 12       | 11             | 10                  | 9                 | 8  |
| HW_LOCK_ILIMIT_MODE | HW_LOCK_ILIMIT_DEG |            |          |                | MIN_VM_MOTOR        |                   |    |
| R/W-0h              | R/W-0h             |            |          |                | R/W-0h              |                   |    |
| 7                   | 6                  | 5          | 4        | 3              | 2                   | 1                 | 0  |
| MIN_VM_MODE         | MAX_VM_MOTOR       |            |          | MAX_VM_MODE    | AUTO_RETRY_TIMES    |                   |    |
| R/W-0h              | R/W-0h             |            |          | R/W-0h         | R/W-0h              |                   |    |

表 7-32. FAULT\_CONFIG2 Register Field Descriptions

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 31    | PARITY         | R/W  | 0h    | Parity bit   |
| 30    | LOCK1_EN       | R/W  | 0h    | Lock 1 : Abnormal speed enable<br>0h = Disable<br>1h = Enable  |
| 29    | LOCK2_EN       | R/W  | 0h    | Lock 2 : Abnormal BEMF enable<br>0h = Disable<br>1h = Enable   |
| 28    | LOCK3_EN       | R/W  | 0h    | Lock 3 : No motor enable<br>0h = Disable<br>1h = Enable  |
| 27-25 | LOCK_ABN_SPEED | R/W  | 0h    | Abnormal speed lock threshold (% of MAX_SPEED)<br>0h = 130%<br>1h = 140%<br>2h = 150%<br>3h = 160%<br>4h = 170%<br>5h = 180%<br>6h = 190%<br>7h = 200% |

表 7-32. FAULT\_CONFIG2 Register Field Descriptions (continued)

| Bit   | Field             | Type | Reset | Description   |
|-------|-------------------|------|-------|---|
| 24-22 | ABNORMAL_BEMF_THR | R/W  | 0h    | Abnormal BEMF lock threshold (% of expected BEMF)<br>0h = 10%<br>1h = 20%<br>2h = 30%<br>3h = 40%<br>4h = 50%<br>5h = 60%<br>6h = 70%<br>7h = 80% |
| 21-19 | NO_MTR_THR        | R/W  | 0h    | No motor lock threshold<br>0h = 0.05 A<br>1h = 0.075 A<br>2h = 0.1 A<br>3h = 0.125 A<br>4h = 0.25 A<br>5h = 0.5 A<br>6h = 0.75 A<br>7h = 1.0 A    |



**表 7-32. FAULT\_CONFIG2 Register Field Descriptions (continued)**

| Bit   | Field               | Type | Reset | Description  |
|-------|---------------------|------|-------|--|
| 18-15 | HW_LOCK_ILIMIT_MODE | R/W  | 0h    | Hardware lock detection current mode<br>0h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated<br>1h = Hardware Ilimit lock detection causes latched fault; nFAULTactive; Gate driver is in recirculation mode<br>2h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON)<br>3h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON)<br>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated<br>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode<br>6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high-side brake mode (All high-side FETs are turned ON)<br>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low-side brake mode (All low-side FETs are turned ON)<br>8h = Hardware Ilimit lock detection is in report only but no action is taken<br>9h = Hardware Ilimit lock detection is disabled<br>Ah = Hardware Ilimit lock detection is disabled<br>Bh = Hardware Ilimit lock detection is disabled<br>Ch = Hardware Ilimit lock detection is disabled<br>Dh = Hardware Ilimit lock detection is disabled<br>Eh = Hardware Ilimit lock detection is disabled<br>Fh = Hardware Ilimit lock detection is disabled |
| 14-11 | HW_LOCK_ILIMIT_DEG  | R/W  | 0h    | Hardware lock detection current limit deglitch time<br>0h = No Deglitch<br>1h = 1 $\mu$ s<br>2h = 2 $\mu$ s<br>3h = 3 $\mu$ s<br>4h = 4 $\mu$ s<br>5h = 5 $\mu$ s<br>6h = 6 $\mu$ s<br>7h = 7 $\mu$ s<br>8h = 8 $\mu$ s<br>9h = 9 $\mu$ s<br>Ah = 10 $\mu$ s<br>Bh = 11 $\mu$ s<br>Ch = 12 $\mu$ s<br>Dh = 13 $\mu$ s<br>Eh = 14 $\mu$ s<br>Fh = 15 $\mu$ s  |

表 7-32. FAULT\_CONFIG2 Register Field Descriptions (continued)

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 10-8 | MIN_VM_MOTOR     | R/W  | 0h    | Minimum voltage for running motor<br>0h = No Limit<br>1h = 4.5 V<br>2h = 5 V<br>3h = 5.5 V<br>4h = 6 V<br>5h = 7.5 V<br>6h = 10 V<br>7h = 12.5 V    |
| 7    | MIN_VM_MODE      | R/W  | 0h    | Undervoltage fault mode<br>0h = Latch on Undervoltage<br>1h = Automatic clear if voltage in bounds  |
| 6-4  | MAX_VM_MOTOR     | R/W  | 0h    | Maximum voltage for running motor<br>0h = No Limit<br>1h = 20 V<br>2h = 22.5 V<br>3h = 25 V<br>4h = 27.5 V<br>5h = 30 V<br>6h = 32.5 V<br>7h = 35 V |
| 3    | MAX_VM_MODE      | R/W  | 0h    | Overvoltage fault mode<br>0h = Latch on Overvoltage<br>1h = Automatic clear if voltage in bounds  |
| 2-0  | AUTO_RETRY_TIMES | R/W  | 0h    | Automatic retry attempts<br>0h = No Limit<br>1h = 2<br>2h = 3<br>3h = 5<br>4h = 7<br>5h = 10<br>6h = 15<br>7h = 20                                  |

### 7.7.3 Hardware\_Configuration Registers

[HARDWARE\\_CONFIGURATION Registers](#) lists the memory-mapped registers for the Hardware\_Configuration registers. All register offset addresses not listed in [HARDWARE\\_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

表 7-33. HARDWARE\_CONFIGURATION Registers

| Address | Acronym        | Register Name               | Section                   |
|---------|----------------|-----------------------------|---------------------------|
| A4h     | PIN_CONFIG     | Hardware Pin Configuration  | <a href="#">节 7.7.3.1</a> |
| A6h     | DEVICE_CONFIG1 | Device Configuration 1      | <a href="#">节 7.7.3.2</a> |
| A8h     | DEVICE_CONFIG2 | Device Configuration 2      | <a href="#">节 7.7.3.3</a> |
| AAh     | PERI_CONFIG1   | Peripheral Configuration 1  | <a href="#">节 7.7.3.4</a> |
| ACH     | GD_CONFIG1     | Gate Driver Configuration 1 | <a href="#">节 7.7.3.5</a> |
| Aeh     | GD_CONFIG2     | Gate Driver Configuration 2 | <a href="#">节 7.7.3.6</a> |

Complex bit access types are encoded to fit into small table cells. [Hardware\\_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

**表 7-34. Hardware\_Configuration Access Type Codes**

| Access Type                   | Code    | Description                            |
|-------------------------------|---------|--|
| <b>Read Type</b>              |         |  |
| R                             | R       | Read                                   |
| <b>Write Type</b>             |         |  |
| W                             | W       | Write                                  |
| W1C                           | W<br>1C | Write<br>1 to clear                    |
| <b>Reset or Default Value</b> |         |  |
| -n                            |         | Value after reset or the default value |

**7.7.3.1 PIN\_CONFIG Register (Address = A4h) [Reset = 0000000h]**

 PIN\_CONFIG is shown in [PIN\\_CONFIG Register](#) and described in [PIN\\_CONFIG Register Field Descriptions](#).

 Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to configure hardware pins

**图 7-71. PIN\_CONFIG Register**

|          |    |                    |                           |             |    |            |    |
|----------|----|--------------------|---------------------------|-------------|----|------------|----|
| 31       | 30 | 29                 | 28                        | 27          | 26 | 25         | 24 |
| PARITY   |    | RESERVED           |                           |             |    |            |    |
| R/W-0h   |    | R/W-0h             |                           |             |    |            |    |
| 23       | 22 | 21                 | 20                        | 19          | 18 | 17         | 16 |
| RESERVED |    |                    |                           |             |    |            |    |
| R/W-0h   |    |                    |                           |             |    |            |    |
| 15       | 14 | 13                 | 12                        | 11          | 10 | 9          | 8  |
| RESERVED |    |                    |                           |             |    |            |    |
| R/W-0h   |    |                    |                           |             |    |            |    |
| 7        | 6  | 5                  | 4                         | 3           | 2  | 1          | 0  |
| RESERVED |    | BRAKE_PIN_M<br>ODE | ALIGN_BRAKE<br>_ANGLE_SEL | BRAKE_INPUT |    | SPEED_MODE |    |
| R/W-0h   |    | R/W-0h             | R/W-0h                    | R/W-0h      |    | R/W-0h     |    |

**表 7-35. PIN\_CONFIG Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description   |
|------|-----------------------|------|-------|---|
| 31   | PARITY                | R/W  | 0h    | Parity bit  |
| 30-6 | RESERVED              | R/W  | 0h    | Reserved  |
| 5    | BRAKE_PIN_MODE        | R/W  | 0h    | Brake pin mode<br>0h = Low side Brake<br>1h = Align Brake   |
| 4    | ALIGN_BRAKE_ANGLE_SEL | R/W  | 0h    | Align brake angle select<br>0h = Use last commutation angle before entering align braking<br>1h = Use ALIGN_ANGLE configuration for align braking   |
| 3-2  | BRAKE_INPUT           | R/W  | 0h    | Brake pin override<br>0h = Hardware Pin BRAKE<br>1h = Override pin and brake / align according to BRAKE_PIN_MODE<br>2h = Override pin and do not brake / align<br>3h = Hardware Pin BRAKE             |
| 1-0  | SPEED_MODE            | R/W  | 0h    | Configure speed control mode from speed pin<br>0h = Analog Mode<br>1h = Controlled by Duty Cycle of SPEED Input Pin<br>2h = Register Override mode<br>3h = Controlled by Frequency of SPEED Input Pin |

### 7.7.3.2 DEVICE\_CONFIG1 Register (Address = A6h) [Reset = X]

DEVICE\_CONFIG1 is shown in [DEVICE\\_CONFIG1 Register](#) and described in [DEVICE\\_CONFIG1 Register Field Descriptions](#).

Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to configure device

**图 7-72. DEVICE\_CONFIG1 Register**

|                 |          |               |          |          |                 |          |    |
|-----------------|----------|---------------|----------|----------|-----------------|----------|----|
| 31              | 30       | 29            | 28       | 27       | 26              | 25       | 24 |
| PARITY          | RESERVED | PIN_38_CONFIG |          | RESERVED | I2C_TARGET_ADDR |          |    |
| R/W-0h          | R/W-0h   | R/W-0h        |          | R/W-0h   | R/W-X           |          |    |
| 23              | 22       | 21            | 20       | 19       | 18              | 17       | 16 |
| I2C_TARGET_ADDR |          |               |          | RESERVED |                 |          |    |
| R/W-X           |          |               |          | R/W-X    |                 |          |    |
| 15              | 14       | 13            | 12       | 11       | 10              | 9        | 8  |
| RESERVED        |          |               |          |          |                 |          |    |
| R/W-X           |          |               |          |          |                 |          |    |
| 7               | 6        | 5             | 4        | 3        | 2               | 1        | 0  |
| RESERVED        |          |               | RESERVED |          |                 | BUS_VOLT |    |
| R/W-X           |          |               | R/W-0h   |          |                 | R/W-0h   |    |

**表 7-36. DEVICE\_CONFIG1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description  |
|-------|-----------------|------|-------|--|
| 31    | PARITY          | R/W  | 0h    | Parity bit   |
| 30    | RESERVED        | R/W  | 0h    | Reserved   |
| 29-28 | PIN_38_CONFIG   | R/W  | 0h    | Pin 38 configuration<br>0h = N/A<br>1h = SOA<br>2h = SOB<br>3h = SOC                         |
| 27    | RESERVED        | R/W  | 0h    | Reserved   |
| 26-20 | I2C_TARGET_ADDR | R/W  | X     | I2C target address   |
| 19-5  | RESERVED        | R/W  | X     | Reserved   |
| 4-2   | RESERVED        | R/W  | 0h    | Reserved   |
| 1-0   | BUS_VOLT        | R/W  | 0h    | Maximum bus voltage configuration<br>0h = 15 V<br>1h = 30 V<br>2h = 60 V<br>3h = Not defined |

### 7.7.3.3 DEVICE\_CONFIG2 Register (Address = A8h) [Reset = 0000000h]

DEVICE\_CONFIG2 is shown in [DEVICE\\_CONFIG2 Register](#) and described in [DEVICE\\_CONFIG2 Register Field Descriptions](#).

Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to configure device

**图 7-73. DEVICE\_CONFIG2 Register**

|                    |    |                     |                         |               |         |              |              |
|--------------------|----|---------------------|-------------------------|---------------|---------|--------------|--------------|
| 31                 | 30 | 29                  | 28                      | 27            | 26      | 25           | 24           |
| PARITY             |    | INPUT_MAXIMUM_FREQ  |                         |               |         |              |              |
| R/W-0h             |    | R/W-0h              |                         |               |         |              |              |
| 23                 | 22 | 21                  | 20                      | 19            | 18      | 17           | 16           |
| INPUT_MAXIMUM_FREQ |    |                     |                         |               |         |              |              |
| R/W-0h             |    |                     |                         |               |         |              |              |
| 15                 | 14 | 13                  | 12                      | 11            | 10      | 9            | 8            |
| SLEEP_ENTRY_TIME   |    | DYNAMIC_CSA_GAIN_EN | DYNAMIC_VOLTAGE_GAIN_EN | DEV_MODE      | CLK_SEL |              | EXT_CLK_EN   |
| R/W-0h             |    | R/W-0h              | R/W-0h                  | R/W-0h        | R/W-0h  |              | R/W-0h       |
| 7                  | 6  | 5                   | 4                       | 3             | 2       | 1            | 0            |
| EXT_CLK_CONFIG     |    |                     | EXT_WD_EN               | EXT_WD_CONFIG |         | EXT_WD_INPUT | EXT_WD_FAULT |
| R/W-0h             |    |                     | R/W-0h                  | R/W-0h        |         | R/W-0h       | R/W-0h       |

**表 7-37. DEVICE\_CONFIG2 Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description   |
|-------|-------------------------|------|-------|---|
| 31    | PARITY                  | R/W  | 0h    | Parity bit  |
| 30-16 | INPUT_MAXIMUM_FREQ      | R/W  | 0h    | Input frequency on speed pin for speed control mode as "controlled by frequency speed pin input" that corresponds to 100% duty cycle. Input duty cycle = Input frequency / INPUT_MAXIMUM_FREQ |
| 15-14 | SLEEP_ENTRY_TIME        | R/W  | 0h    | Device enters sleep mode when speed input is held continuously below the speed threshold for SEEP_ENTRY_TIME<br>0h = 50 µs<br>1h = 200 µs<br>2h = 20 ms<br>3h = 200 ms                        |
| 13    | DYNAMIC_CSA_GAIN_EN     | R/W  | 0h    | Adjust CSA gain at 1ms rate for optimal current resolution at all current levels<br>0h = Disable<br>1h = Enable   |
| 12    | DYNAMIC_VOLTAGE_GAIN_EN | R/W  | 0h    | Adjust voltage gain at 1ms rate for optimal voltage resolution at all voltage levels<br>0h = Dynamic Voltage Gain is Disabled<br>1h = Dynamic Voltage Gain is Enabled                         |
| 11    | DEV_MODE                | R/W  | 0h    | Device mode select<br>0h = Standby Mode<br>1h = Sleep Mode  |
| 10-9  | CLK_SEL                 | R/W  | 0h    | Clock source<br>0h = Internal Oscillator<br>1h = N/A<br>2h = N/A<br>3h = External Clock input   |

**表 7-37. DEVICE\_CONFIG2 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 8   | EXT_CLK_EN     | R/W  | 0h    | External clock mode enable<br>0h = Disable<br>1h = Enable   |
| 7-5 | EXT_CLK_CONFIG | R/W  | 0h    | External clock configuration<br>0h = 8 kHz<br>1h = 16 kHz<br>2h = 32 kHz<br>3h = 64 kHz<br>4h = 128 kHz<br>5h = 256 kHz<br>6h = 512 kHz<br>7h = 1024 kHz  |
| 4   | EXT_WD_EN      | R/W  | 0h    | External watchdog enable<br>0h = Disable<br>1h = Enable   |
| 3-2 | EXT_WD_CONFIG  | R/W  | 0h    | Time between watchdog tickles<br>0h = 100ms if GPIO mode; 1s if I2C mode<br>1h = 200ms if GPIO mode; 2s if I2C mode<br>2h = 500ms if GPIO mode; 5s if I2C mode<br>3h = 1000ms if GPIO mode; 10s if I2C mode |
| 1   | EXT_WD_INPUT   | R/W  | 0h    | External watchdog input mode<br>0h = Watchdog tickle over I2C<br>1h = Watchdog tickle over GPIO   |
| 0   | EXT_WD_FAULT   | R/W  | 0h    | External watchdog fault mode<br>0h = Report Only<br>1h = Latch with Hi-Z outputs  |

**7.7.3.4 PERI\_CONFIG1 Register (Address = AAh) [Reset = 4000000h]**

PERI\_CONFIG1 is shown in [PERI\\_CONFIG1 Register](#) and described in [PERI\\_CONFIG1 Register Field Descriptions](#).

Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to peripheral1

**图 7-74. PERI\_CONFIG1 Register**

| 31                             | 30                             | 29        | 28                           | 27              | 26               | 25                             | 24            |
|--------------------------------|--------------------------------|-----------|------------------------------|-----------------|------------------|--------------------------------|---------------|
| PARITY                         | SPREAD_SPECTRUM_MODULATION_DIS | RESERVED  |                              |                 |                  | BUS_CURRENT_LIMIT              |               |
| R/W-0h                         | R/W-1h                         | R/W-0h    |                              |                 |                  | R/W-0h                         |               |
| 23                             | 22                             | 21        | 20                           | 19              | 18               | 17                             | 16            |
| BUS_CURRENT_LIMIT              | BUS_CURRENT_LIMIT_ENABLE       | DIR_INPUT |                              | DIR_CHANGE_MODE | SELF_TEST_ENABLE | ACTIVE_BRAKE_SPEED_DELTA_LIMIT |               |
| R/W-0h                         | R/W-0h                         | R/W-0h    |                              | R/W-0h          | R/W-0h           | R/W-0h                         | R/W-0h        |
| 15                             | 14                             | 13        | 12                           | 11              | 10               | 9                              | 8             |
| ACTIVE_BRAKE_SPEED_DELTA_LIMIT |                                |           | ACTIVE_BRAKE_MOD_INDEX_LIMIT |                 |                  | SPEED_RANGE_SEL                | ALARM_PIN_DIS |
| R/W-0h                         |                                |           | R/W-0h                       |                 |                  | R/W-0h                         | R/W-0h        |
| 7                              | 6                              | 5         | 4                            | 3               | 2                | 1                              | 0             |
| RESERVED                       |                                |           |                              |                 |                  |                                |               |
| R/W-0h                         |                                |           |                              |                 |                  |                                |               |

**表 7-38. PERI\_CONFIG1 Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description  |
|-------|--------------------------------|------|-------|--|
| 31    | PARITY                         | R/W  | 0h    | Parity bit   |
| 30    | SPREAD_SPECTRUM_MODULATION_DIS | R/W  | 1h    | Spread spectrum modulation disable<br>0h = SSM is Enabled<br>1h = SSM is Disabled  |
| 29-26 | RESERVED                       | R/W  | 0h    | Reserved   |
| 25-22 | BUS_CURRENT_LIMIT              | R/W  | 0h    | Bus current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |



**表 7-38. PERI\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field                          | Type | Reset | Description   |
|-------|--------------------------------|------|-------|---|
| 21    | BUS_CURRENT_LIMIT_ENABLE       | R/W  | 0h    | Bus current limit enable<br>0h = Disable<br>1h = Enable   |
| 20-19 | DIR_INPUT                      | R/W  | 0h    | DIR pin override<br>0h = Hardware Pin DIR<br>1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC<br>2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB<br>3h = Hardware Pin DIR  |
| 18    | DIR_CHANGE_MODE                | R/W  | 0h    | Response to change of DIR pin status<br>0h = Follow motor stop options and ISD routine on detecting DIR change<br>1h = Change the direction through Reverse Drive while continuously driving the motor  |
| 17    | SELF_TEST_ENABLE               | R/W  | 0h    | Self-test on power up enable<br>0h = STL is disabled<br>1h = STL is enabled   |
| 16-13 | ACTIVE_BRAKE_SPEED_DELTA_LIMIT | R/W  | 0h    | Difference between final speed and present speed beyond which active braking will be applied<br>0h = 2.5%<br>1h = 5%<br>2h = 10%<br>3h = 15%<br>4h = 20%<br>5h = 25%<br>6h = 30%<br>7h = 35%<br>8h = 40%<br>9h = 45%<br>Ah = 50%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 12-10 | ACTIVE_BRAKE_MOD_INDEX_LIMIT   | R/W  | 0h    | Modulation index limit beyond which active braking will be applied<br>0h = 0%<br>1h = 40%<br>2h = 50%<br>3h = 60%<br>4h = 70%<br>5h = 80%<br>6h = 90%<br>7h = 100%  |
| 9     | SPEED_RANGE_SEL                | R/W  | 0h    | Speed range selection for digital speed (PWM duty or frequency to speed mode)<br>0h = 325 Hz to 95 kHz<br>1h = 10 Hz to 325 Hz  |
| 8     | ALARM_PIN_DIS                  | R/W  | 0h    | Alarm pin disable<br>0h = Alarm pin is enabled<br>1h = Alarm pin is disabled  |

表 7-38. PERI\_CONFIG1 Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-0 | RESERVED | R/W  | 0h    | Reserved    |

### 7.7.3.5 GD\_CONFIG1 Register (Address = ACh) [Reset = 10228100h]

GD\_CONFIG1 is shown in [GD\\_CONFIG1 Register](#) and described in [GD\\_CONFIG1 Register Field Descriptions](#).  
Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to configure gated driver settings1

**图 7-75. GD\_CONFIG1 Register**

|          |  |          |  |          |  |          |  |           |  |          |  |          |  |         |  |
|----------|--|----------|--|----------|--|----------|--|-----------|--|----------|--|----------|--|---------|--|
| 31       |  | 30       |  | 29       |  | 28       |  | 27        |  | 26       |  | 25       |  | 24      |  |
| PARITY   |  | RESERVED |  |          |  | RESERVED |  | SLEW_RATE |  |          |  | RESERVED |  |         |  |
| R/W-0h   |  | R/W-0h   |  |          |  | R/W-1h   |  | R/W-0h    |  |          |  | R/W-0h   |  |         |  |
| 23       |  | 22       |  | 21       |  | 20       |  | 19        |  | 18       |  | 17       |  | 16      |  |
| RESERVED |  | RESERVED |  | RESERVED |  | RESERVED |  | OVP_SEL   |  | OVP_EN   |  | RESERVED |  | OTW_REP |  |
| R/W-0h   |  | R/W-0h   |  | R/W-1h   |  | R/W-0h   |  | R/W-0h    |  | R/W-0h   |  | R/W-1h   |  | R/W-0h  |  |
| 15       |  | 14       |  | 13       |  | 12       |  | 11        |  | 10       |  | 9        |  | 8       |  |
| RESERVED |  | RESERVED |  | OCP_DEG  |  |          |  | TRETRY    |  | OCP_LVL  |  | OCP_MODE |  |         |  |
| R/W-1h   |  | R/W-0h   |  | R/W-0h   |  |          |  | R/W-0h    |  | R/W-0h   |  | R/W-1h   |  |         |  |
| 7        |  | 6        |  | 5        |  | 4        |  | 3         |  | 2        |  | 1        |  | 0       |  |
| RESERVED |  | RESERVED |  | RESERVED |  | RESERVED |  | RESERVED  |  | RESERVED |  | CSA_GAIN |  |         |  |
| R/W-0h   |  | R/W-0h   |  | R/W-0h   |  | R/W-0h   |  | R/W-0h    |  | R/W-0h   |  | R/W-0h   |  |         |  |

**表 7-39. GD\_CONFIG1 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 31    | PARITY    | R/W  | 0h    | Parity bit   |
| 30-29 | RESERVED  | R/W  | 0h    | Reserved   |
| 28    | RESERVED  | R/W  | 1h    | Reserved   |
| 27-26 | SLEW_RATE | R/W  | 0h    | Slew rate<br>0h = Slew rate is 25 V/μs<br>1h = Slew rate is 50 V/μs<br>2h = Slew rate is 150 V/μs<br>3h = Slew rate is 200 V/μs                              |
| 25-24 | RESERVED  | R/W  | 0h    | Reserved   |
| 23    | RESERVED  | R/W  | 0h    | Reserved   |
| 22    | RESERVED  | R/W  | 0h    | Reserved   |
| 21    | RESERVED  | R/W  | 1h    | Reserved   |
| 20    | RESERVED  | R/W  | 0h    | Reserved   |
| 19    | OVP_SEL   | R/W  | 0h    | Overvoltage protection level<br>0h = VM overvoltage level is 32-V<br>1h = VM overvoltage level is 20-V   |
| 18    | OVP_EN    | R/W  | 0h    | Overvoltage protection enable<br>0h = Overvoltage protection is disabled<br>1h = Overvoltage protection is enabled   |
| 17    | RESERVED  | R/W  | 1h    | Reserved   |
| 16    | OTW_REP   | R/W  | 0h    | Overtemperature warning reporting on nFAULT<br>0h = Over temperature reporting on nFAULT is disabled<br>1h = Over temperature reporting on nFAULT is enabled |
| 15    | RESERVED  | R/W  | 1h    | Reserved   |
| 14    | RESERVED  | R/W  | 0h    | Reserved   |

表 7-39. GD\_CONFIG1 Register Field Descriptions (continued)

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 13-12 | OCF_DEG  | R/W  | 0h    | OCF deglitch time<br>0h = OCF deglitch time is 0.2 $\mu$ s<br>1h = OCF deglitch time is 0.6 $\mu$ s<br>2h = OCF deglitch time is 1.1 $\mu$ s<br>3h = OCF deglitch time is 1.6 $\mu$ s   |
| 11    | TRETRY   | R/W  | 0h    | OCF retry time<br>0h = OCF retry time is 5 ms<br>1h = OCF retry time is 500 ms  |
| 10    | OCF_LVL  | R/W  | 0h    | OCF level<br>0h = OCF level is 16 A (Typical)<br>1h = OCF level is 24 A (Typical)   |
| 9-8   | OCF_MODE | R/W  | 1h    | OCF fault mode<br>0h = Overcurrent causes a latched fault<br>1h = Overcurrent causes an automatic retrying fault<br>2h = Overcurrent is report only but no action is taken<br>3h = Overcurrent is not reported and no action is taken |
| 7     | RESERVED | R/W  | 0h    | Reserved  |
| 6     | RESERVED | R/W  | 0h    | Reserved  |
| 5     | RESERVED | R/W  | 0h    | Reserved  |
| 4     | RESERVED | R/W  | 0h    | Reserved  |
| 3     | RESERVED | R/W  | 0h    | Reserved  |
| 2     | RESERVED | R/W  | 0h    | Reserved  |
| 1-0   | CSA_GAIN | R/W  | 0h    | Current Sense Amplifier (CSA) gain (used only if DYNAMIC_CSA_GAIN_EN = 0)<br>0h = CSA gain is 0.15 V/A<br>1h = CSA gain is 0.3 V/A<br>2h = CSA gain is 0.6 V/A<br>3h = CSA gain is 1.2 V/A  |

### 7.7.3.6 GD\_CONFIG2 Register (Address = AEh) [Reset = 0120000h]

GD\_CONFIG2 is shown in [GD\\_CONFIG2 Register](#) and described in [GD\\_CONFIG2 Register Field Descriptions](#).  
Return to the [HARDWARE\\_CONFIGURATION Registers](#).

Register to configure gated driver settings2

图 7-76. GD\_CONFIG2 Register

|          |               |              |          |          |    |         |             |
|----------|---------------|--------------|----------|----------|----|---------|-------------|
| 31       | 30            | 29           | 28       | 27       | 26 | 25      | 24          |
| PARITY   | DELAY_COMP_EN | TARGET_DELAY |          |          |    | BUCK_SR | BUCK_PS_DIS |
| R/W-0h   | R/W-0h        | R/W-0h       |          |          |    | R/W-0h  | R/W1C-1h    |
| 23       | 22            | 21           | 20       | 19       | 18 | 17      | 16          |
| BUCK_CL  | BUCK_SEL      |              | BUCK_DIS | RESERVED |    |         |             |
| R/W-0h   | R/W-1h        |              | R/W-0h   | R/W-0h   |    |         |             |
| 15       | 14            | 13           | 12       | 11       | 10 | 9       | 8           |
| RESERVED |               |              |          |          |    |         |             |
| R/W-0h   |               |              |          |          |    |         |             |
| 7        | 6             | 5            | 4        | 3        | 2  | 1       | 0           |
| RESERVED |               |              |          |          |    |         |             |
| R/W-0h   |               |              |          |          |    |         |             |

表 7-40. GD\_CONFIG2 Register Field Descriptions

| Bit   | Field         | Type  | Reset | Description   |
|-------|---------------|-------|-------|---|
| 31    | PARITY        | R/W   | 0h    | Parity bit  |
| 30    | DELAY_COMP_EN | R/W   | 0h    | Driver delay compensation enable<br>0h = Disable<br>1h = Enable   |
| 29-26 | TARGET_DELAY  | R/W   | 0h    | Target delay<br>0h = Automatic based on slew rate<br>1h = 0.4 $\mu$ s<br>2h = 0.6 $\mu$ s<br>3h = 0.8 $\mu$ s<br>4h = 1 $\mu$ s<br>5h = 1.2 $\mu$ s<br>6h = 1.4 $\mu$ s<br>7h = 1.6 $\mu$ s<br>8h = 1.8 $\mu$ s<br>9h = 2 $\mu$ s<br>Ah = 2.2 $\mu$ s<br>Bh = 2.4 $\mu$ s<br>Ch = 2.6 $\mu$ s<br>Dh = 2.8 $\mu$ s<br>Eh = 3 $\mu$ s<br>Fh = 3.2 $\mu$ s |
| 25    | BUCK_SR       | R/W   | 0h    | Buck slew rate<br>0h = Buck's FET slew rate is 1000V/ $\mu$ s<br>1h = Buck's FET slew rate is 200V/ $\mu$ s   |
| 24    | BUCK_PS_DIS   | R/W1C | 1h    | Buck power sequencing disable<br>0h = Buck power sequencing is enabled<br>1h = Buck power sequencing is disabled  |

表 7-40. GD\_CONFIG2 Register Field Descriptions (continued)

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 23    | BUCK_CL  | R/W  | 0h    | Buck current limit<br>0h = Buck regulator current limit is set to 600 mA<br>1h = Buck regulator current limit is set to 150 mA                 |
| 22-21 | BUCK_SEL | R/W  | 1h    | Buck voltage selection<br>0h = Buck voltage is 3.3 V<br>1h = Buck voltage is 5.0 V<br>2h = Buck voltage is 4.0 V<br>3h = Buck voltage is 5.7 V |
| 20    | BUCK_DIS | R/W  | 0h    | Buck disable<br>0h = Buck regulator is enabled<br>1h = Buck regulator is disabled  |
| 19-0  | RESERVED | R/W  | 0h    | Reserved   |

### 7.7.4 Internal\_Algorithm\_Configuration Registers

[INTERNAL\\_ALGORITHM\\_CONFIGURATION Registers](#) lists the memory-mapped registers for the Internal\_Algorithm\_Configuration registers. All register offset addresses not listed in [INTERNAL\\_ALGORITHM\\_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

表 7-41. INTERNAL\_ALGORITHM\_CONFIGURATION Registers

| Address | Acronym    | Register Name                      | Section                   |
|---------|------------|------------------------------------|---------------------------|
| A0h     | INT_ALGO_1 | Internal Algorithm Configuration 1 | <a href="#">节 7.7.4.1</a> |
| A2h     | INT_ALGO_2 | Internal Algorithm Configuration 2 | <a href="#">节 7.7.4.2</a> |

Complex bit access types are encoded to fit into small table cells. [Internal\\_Algorithm\\_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

表 7-42. Internal\_Algorithm\_Configuration Access Type Codes

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Write Type</b>             |      |  |
| W                             | W    | Write                                  |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

### 7.7.4.1 INT\_ALGO\_1 Register (Address = A0h) [Reset = X]

INT\_ALGO\_1 is shown in [INT\\_ALGO\\_1 Register](#) and described in [INT\\_ALGO\\_1 Register Field Descriptions](#).  
Return to the [INTERNAL\\_ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure internal algorithm parameters1

**图 7-77. INT\_ALGO\_1 Register**

|                          |  |                          |  |                                 |  |                            |  |             |  |               |  |        |  |        |  |
|--------------------------|--|--------------------------|--|---------------------------------|--|----------------------------|--|-------------|--|---------------|--|--------|--|--------|--|
| 31                       |  | 30                       |  | 29                              |  | 28                         |  | 27          |  | 26            |  | 25     |  | 24     |  |
| PARITY                   |  | RESERVED                 |  | FG_ANGLE_IN<br>TERPOLATE_E<br>N |  | SPEED_PIN_GLITCH_FILTER    |  | FAST_ISD_EN |  | ISD_STOP_TIME |  |        |  |        |  |
| R/W-0h                   |  | R/W-X                    |  | R/W-0h                          |  | R/W-0h                     |  | R/W-0h      |  | R/W-0h        |  | R/W-0h |  | R/W-0h |  |
| 23                       |  | 22                       |  | 21                              |  | 20                         |  | 19          |  | 18            |  | 17     |  | 16     |  |
| ISD_RUN_TIME             |  | ISD_TIMEOUT              |  | AUTO_HANDOFF_MIN_BEMF           |  | RESERVED                   |  |             |  |               |  |        |  |        |  |
| R/W-0h                   |  | R/W-0h                   |  | R/W-0h                          |  | R/W-0h                     |  | R/W-0h      |  | R/W-0h        |  | R/W-0h |  | R/W-0h |  |
| 15                       |  | 14                       |  | 13                              |  | 12                         |  | 11          |  | 10            |  | 9      |  | 8      |  |
| RESERVED                 |  | MPET_IPD_CURRENT_LIMIT   |  | MPET_IPD_FREQ                   |  | MPET_OPEN_LOOP_CURRENT_REF |  |             |  |               |  |        |  |        |  |
| R/W-0h                   |  | R/W-0h                   |  | R/W-0h                          |  | R/W-0h                     |  | R/W-0h      |  | R/W-0h        |  | R/W-0h |  | R/W-0h |  |
| 7                        |  | 6                        |  | 5                               |  | 4                          |  | 3           |  | 2             |  | 1      |  | 0      |  |
| MPET_OPEN_LOOP_SPEED_REF |  | MPET_OPEN_LOOP_SLEW_RATE |  | REV_DRV_OPEN_LOOP_DEC           |  |                            |  |             |  |               |  |        |  |        |  |
| R/W-0h                   |  | R/W-0h                   |  | R/W-0h                          |  | R/W-0h                     |  | R/W-0h      |  | R/W-0h        |  | R/W-0h |  | R/W-0h |  |

**表 7-43. INT\_ALGO\_1 Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description   |
|-------|-------------------------|------|-------|---|
| 31    | PARITY                  | R/W  | 0h    | Parity bit  |
| 30    | RESERVED                | R/W  | X     | Reserved  |
| 29    | FG_ANGLE_INTERPOLATE_EN | R/W  | 0h    | Angle interpolation for FG enable<br>0h = Disable<br>1h = Enable  |
| 28-27 | SPEED_PIN_GLITCH_FILTER | R/W  | 0h    | Glitch filter applied on speed pin input<br>0h = No Glitch Filter<br>1h = 0.2 $\mu$ s<br>2h = 0.5 $\mu$ s<br>3h = 1.0 $\mu$ s |
| 26    | FAST_ISD_EN             | R/W  | 0h    | Fast initial speed detection enable<br>0h = Disable Fast ISD<br>1h = Enable Fast ISD  |
| 25-24 | ISD_STOP_TIME           | R/W  | 0h    | Persistence time for declaring motor has stopped<br>0h = 1 ms<br>1h = 5 ms<br>2h = 50 ms<br>3h = 100 ms                       |
| 23-22 | ISD_RUN_TIME            | R/W  | 0h    | Persistence time for declaring motor is running<br>0h = 1 ms<br>1h = 5 ms<br>2h = 50 ms<br>3h = 100 ms                        |

表 7-43. INT\_ALGO\_1 Register Field Descriptions (continued)

| Bit   | Field                      | Type | Reset | Description   |
|-------|----------------------------|------|-------|---|
| 21-20 | ISD_TIMEOUT                | R/W  | 0h    | Timeout in case ISD is unable to reliably detect speed or direction<br>0h = 500ms<br>1h = 750 ms<br>2h = 1000 ms<br>3h = 2000 ms                                  |
| 19-17 | AUTO_HANDOFF_MIN_BEMF      | R/W  | 0h    | Minimum BEMF for handoff<br>0h = 0 mV<br>1h = 50 mV<br>2h = 100 mV<br>3h = 250 mV<br>4h = 500 mV<br>5h = 1000 mV<br>6h = 1250 mV<br>7h = 1500 mV                  |
| 16-15 | RESERVED                   | R/W  | 0h    | Reserved  |
| 14-13 | MPET_IPD_CURRENT_LIMIT     | R/W  | 0h    | IPD current limit for MPET<br>0h = 0.1 A<br>1h = 0.5 A<br>2h = 1.0 A<br>3h = 2.0 A  |
| 12-11 | MPET_IPD_FREQ              | R/W  | 0h    | Number of times IPD is executed for MPET<br>0h = 1<br>1h = 2<br>2h = 4<br>3h = 8  |
| 10-8  | MPET_OPEN_LOOP_CURRENT_REF | R/W  | 0h    | Open loop current reference<br>0h = 1 A<br>1h = 2 A<br>2h = 3 A<br>3h = 4 A<br>4h = 5 A<br>5h = 6 A<br>6h = 7 A<br>7h = 8 A                                       |
| 7-6   | MPET_OPEN_LOOP_SPEED_REF   | R/W  | 0h    | Open loop speed reference for MPET (% of MAXIMUM_SPEED)<br>0h = 15%<br>1h = 25%<br>2h = 35%<br>3h = 50%   |
| 5-3   | MPET_OPEN_LOOP_SLEW_RATE   | R/W  | 0h    | Open loop slew rate for MPET (Hz/s)<br>0h = 0.1 Hz/s<br>1h = 0.5 Hz/s<br>2h = 1 Hz/s<br>3h = 2 Hz/s<br>4h = 3 Hz/s<br>5h = 5 Hz/s<br>6h = 10 Hz/s<br>7h = 20 Hz/s |



**表 7-43. INT\_ALGO\_1 Register Field Descriptions (continued)**

| Bit | Field                 | Type | Reset | Description   |
|-----|-----------------------|------|-------|---|
| 2-0 | REV_DRV_OPEN_LOOP_DEC | R/W  | 0h    | % of open loop acceleration to be applied during open loop deceleration in reverse drive<br>0h = 50%<br>1h = 60%<br>2h = 70%<br>3h = 80%<br>4h = 90%<br>5h = 100%<br>6h = 125%<br>7h = 150% |

### 7.7.4.2 INT\_ALGO\_2 Register (Address = A2h) [Reset = 0000000h]

INT\_ALGO\_2 is shown in [INT\\_ALGO\\_2 Register](#) and described in [INT\\_ALGO\\_2 Register Field Descriptions](#).

Return to the [INTERNAL\\_ALGORITHM\\_CONFIGURATION Registers](#).

Register to configure internal algorithm parameters2

图 7-78. INT\_ALGO\_2 Register

|             |    |                                    |    |    |                 |                                |                        |
|-------------|----|------------------------------------|----|----|-----------------|--------------------------------|------------------------|
| 31          | 30 | 29                                 | 28 | 27 | 26              | 25                             | 24                     |
| PARITY      |    | RESERVED                           |    |    |                 |                                |                        |
| R/W-0h      |    | R/W-0h                             |    |    |                 |                                |                        |
| 23          | 22 | 21                                 | 20 | 19 | 18              | 17                             | 16                     |
| RESERVED    |    |                                    |    |    |                 |                                |                        |
| R/W-0h      |    |                                    |    |    |                 |                                |                        |
| 15          | 14 | 13                                 | 12 | 11 | 10              | 9                              | 8                      |
| RESERVED    |    |                                    |    |    |                 | CL_SLOW_ACC                    |                        |
| R/W-0h      |    |                                    |    |    |                 | R/W-0h                         |                        |
| 7           | 6  | 5                                  | 4  | 3  | 2               | 1                              | 0                      |
| CL_SLOW_ACC |    | ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE |    |    | MPET_IPD_SELECT | MPET_KEY_MEAS_PARAMETER_SELECT | IPD_HIGH_RESOLUTION_EN |
| R/W-0h      |    | R/W-0h                             |    |    | R/W-0h          | R/W-0h                         | R/W-0h                 |

表 7-44. INT\_ALGO\_2 Register Field Descriptions

| Bit   | Field                              | Type | Reset | Description  |
|-------|------------------------------------|------|-------|--|
| 31    | PARITY                             | R/W  | 0h    | Parity bit   |
| 30-10 | RESERVED                           | R/W  | 0h    | Reserved   |
| 9-6   | CL_SLOW_ACC                        | R/W  | 0h    | Close loop acceleration when estimator is not yet fully aligned<br>0h = 0.1 Hz/s<br>1h = 1 Hz/s<br>2h = 2 Hz/s<br>3h = 3 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 20 Hz/s<br>7h = 30 Hz/s<br>8h = 40 Hz/s<br>9h = 50 Hz/s<br>Ah = 100 Hz/s<br>Bh = 200 Hz/s<br>Ch = 500 Hz/s<br>Dh = 750 Hz/s<br>Eh = 1000 Hz/s<br>Fh = 2000 Hz/s |
| 5-3   | ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE | R/W  | 0h    | Bus current slew rate during active braking<br>0h = 10 A/s<br>1h = 50 A/s<br>2h = 100 A/s<br>3h = 250 A/s<br>4h = 500 A/s<br>5h = 1000 A/s<br>6h = 5000 A/s<br>7h = No Limit   |

**表 7-44. INT\_ALGO\_2 Register Field Descriptions (continued)**

| Bit | Field                         | Type | Reset | Description   |
|-----|-------------------------------|------|-------|---|
| 2   | MPET_IPD_SELECT               | R/W  | 0h    | Selection between MPET_IPD_CURRENT_LIMIT for IPD current limit, MPET_IPD_FREQ for IPD Repeat OR IPD_CURR_THR for IPD current limit, IPD_REPEAT for IPD Repeat<br>0h = Configured parameters for normal motor operation<br>1h = MPET specific parameters   |
| 1   | MPET_KE_MEAS_PARAMETER_SELECT | R/W  | 0h    | Selection between MPET_OPEN_LOOP_SLEW_RATE for slew rate, MPET_OPEN_LOOP_CURR_REF for current reference, MPET_OPEN_LOOP_SPEED_REF for speed reference OR OL_ACC_A1, OL_ACC_A2 for slew rate, 80% of ILIMIT for current reference and 50% of MAX_SPEED for speed reference<br>0h = Configured parameters for normal motor operation<br>1h = MPET specific parameters |
| 0   | IPD_HIGH_RESOLUTION_EN        | R/W  | 0h    | IPD high resolution enable<br>0h = Disable<br>1h = Enable   |

## 7.8 RAM (Volatile) Register Map

### 7.8.1 Fault\_Status Registers

[FAULT\\_STATUS Registers](#) lists the memory-mapped registers for the Fault\_Status registers. All register offset addresses not listed in [FAULT\\_STATUS Registers](#) should be considered as reserved locations and the register contents should not be modified.

**表 7-45. FAULT\_STATUS Registers**

| Address | Acronym                  | Register Name         | Section                   |
|---------|--------------------------|-----------------------|---------------------------|
| E0h     | GATE_DRIVER_FAULT_STATUS | Fault Status Register | <a href="#">节 7.8.1.1</a> |
| E2h     | CONTROLLER_FAULT_STATUS  | Fault Status Register | <a href="#">节 7.8.1.2</a> |

Complex bit access types are encoded to fit into small table cells. [Fault\\_Status Access Type Codes](#) shows the codes that are used for access types in this section.

**表 7-46. Fault\_Status Access Type Codes**

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

#### 7.8.1.1 GATE\_DRIVER\_FAULT\_STATUS Register (Address = E0h) [Reset = 0000000h]

GATE\_DRIVER\_FAULT\_STATUS is shown in [GATE\\_DRIVER\\_FAULT\\_STATUS Register](#) and described in [GATE\\_DRIVER\\_FAULT\\_STATUS Register Field Descriptions](#).

Return to the [FAULT\\_STATUS Registers](#).

Status of various gate driver faults

**图 7-79. GATE\_DRIVER\_FAULT\_STATUS Register**

|              |         |          |         |        |          |        |          |
|--------------|---------|----------|---------|--------|----------|--------|----------|
| 31           | 30      | 29       | 28      | 27     | 26       | 25     | 24       |
| DRIVER_FAULT | BK_FLT  | RESERVED | OCP     | NPOR   | OVP      | OT     | RESERVED |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h   | R-0h     | R-0h   | R-0h     |
| 23           | 22      | 21       | 20      | 19     | 18       | 17     | 16       |
| OTW          | TSD     | OCP_HC   | OCP_LC  | OCP_HB | OCP_LB   | OCP_HA | OCP_LA   |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h   | R-0h     | R-0h   | R-0h     |
| 15           | 14      | 13       | 12      | 11     | 10       | 9      | 8        |
| RESERVED     | OTP_ERR | BUCK_OCP | BUCK_UV | VCP_UV | RESERVED |        |          |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h   | R-0h     |        |          |
| 7            | 6       | 5        | 4       | 3      | 2        | 1      | 0        |
| RESERVED     |         |          |         |        |          |        |          |
| R-0h         |         |          |         |        |          |        |          |

**表 7-47. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions**

| Bit | Field        | Type | Reset | Description                        |
|-----|--------------|------|-------|------------------------------------|
| 31  | DRIVER_FAULT | R    | 0h    | Logic OR of driver fault registers |

**表 7-47. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 30  | BK_FLT   | R    | 0h    | Buck fault<br>0h = No buck regulator fault condition is detected<br>1h = Buck regulator fault condition is detected   |
| 29  | RESERVED | R    | 0h    | Reserved  |
| 28  | OCP      | R    | 0h    | Overcurrent protection status<br>0h = No overcurrent condition is detected<br>1h = Overcurrent condition is detected  |
| 27  | NPOR     | R    | 0h    | Supply power on reset<br>0h = Power on reset condition is detected on VM<br>1h = No power-on-reset condition is detected on VM                                      |
| 26  | OVP      | R    | 0h    | Supply overvoltage protection status<br>0h = No overvoltage condition is detected on VM<br>1h = Overvoltage condition is detected on VM                             |
| 25  | OT       | R    | 0h    | Overtemperature fault status<br>0h = No overtemperature warning / shutdown is detected<br>1h = Overtemperature warning / shutdown is detected                       |
| 24  | RESERVED | R    | 0h    | Reserved  |
| 23  | OTW      | R    | 0h    | Overtemperature warning status<br>0h = No overtemperature warning is detected<br>1h = Overtemperature warning is detected   |
| 22  | TSD      | R    | 0h    | Overtemperature shutdown status<br>0h = No overtemperature shutdown is detected<br>1h = Overtemperature shutdown is detected  |
| 21  | OCP_HC   | R    | 0h    | Overcurrent status on high-side switch of OUTC<br>0h = No overcurrent detected on high-side switch of OUTC<br>1h = Overcurrent detected on high-side switch of OUTC |
| 20  | OCP_LC   | R    | 0h    | Overcurrent status on low-side switch of OUTC<br>0h = No overcurrent detected on low-side switch of OUTC<br>1h = Overcurrent detected on low-side switch of OUTC    |
| 19  | OCP_HB   | R    | 0h    | Overcurrent status on high-side switch of OUTB<br>0h = No overcurrent detected on high-side switch of OUTB<br>1h = Overcurrent detected on high-side switch of OUTB |
| 18  | OCP_LB   | R    | 0h    | Overcurrent status on low-side switch of OUTB<br>0h = No overcurrent detected on low-side switch of OUTB<br>1h = Overcurrent detected on low-side switch of OUTB    |
| 17  | OCP_HA   | R    | 0h    | Overcurrent status on high-side switch of OUTA<br>0h = No overcurrent detected on high-side switch of OUTA<br>1h = Overcurrent detected on high-side switch of OUTA |
| 16  | OCP_LA   | R    | 0h    | Overcurrent status on low-side switch of OUTA<br>0h = No overcurrent detected on low-side switch of OUTA<br>1h = Overcurrent detected on low-side switch of OUTA    |
| 15  | RESERVED | R    | 0h    | Reserved  |
| 14  | OTP_ERR  | R    | 0h    | One-time programmable (OTP) error<br>0h = No OTP error is detected<br>1h = OTP Error is detected  |
| 13  | BUCK_OCP | R    | 0h    | Buck regulator overcurrent status<br>0h = No buck regulator overcurrent is detected<br>1h = Buck regulator overcurrent is detected                                  |

**表 7-47. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit  | Field    | Type | Reset | Description   |
|------|----------|------|-------|---|
| 12   | BUCK_UV  | R    | 0h    | Buck regulator undervoltage status<br>0h = No buck regulator undervoltage is detected<br>1h = Buck regulator undervoltage is detected |
| 11   | VCP_UV   | R    | 0h    | Charge pump undervoltage status<br>0h = No charge pump undervoltage is detected<br>1h = Charge pump undervoltage is detected          |
| 10-0 | RESERVED | R    | 0h    | Reserved  |

**7.8.1.2 CONTROLLER\_FAULT\_STATUS Register (Address = E2h) [Reset = 0000000h]**

CONTROLLER\_FAULT\_STATUS is shown in [CONTROLLER\\_FAULT\\_STATUS Register](#) and described in [CONTROLLER\\_FAULT\\_STATUS Register Field Descriptions](#).

Return to the [FAULT\\_STATUS Registers](#).

Status of various controller faults

**图 7-80. CONTROLLER\_FAULT\_STATUS Register**

|                       |                         |                |              |              |                          |                   |                  |
|-----------------------|-------------------------|----------------|--------------|--------------|--------------------------|-------------------|------------------|
| 31                    | 30                      | 29             | 28           | 27           | 26                       | 25                | 24               |
| CONTROLLER_FAULT      | RESERVED                | IPD_FREQ_FAULT | IPD_T1_FAULT | IPD_T2_FAULT | BUS_CURRENT_LIMIT_STATUS | MPET_IPD_FAULT    | MPET_BEMF_FAULT  |
| R-0h                  | R-0h                    | R-0h           | R-0h         | R-0h         | R-0h                     | R-0h              | R-0h             |
| 23                    | 22                      | 21             | 20           | 19           | 18                       | 17                | 16               |
| ABN_SPEED             | ABN_BEMF                | NO_MTR         | MTR_LCK      | LOCK_ILIMIT  | HW_LOCK_ILIMIT           | MTR_UNDER_VOLTAGE | MTR_OVER_VOLTAGE |
| R-0h                  | R-0h                    | R-0h           | R-0h         | R-0h         | R-0h                     | R-0h              | R-0h             |
| 15                    | 14                      | 13             | 12           | 11           | 10                       | 9                 | 8                |
| SPEED_LOOP_SATURATION | CURRENT_LOOP_SATURATION | RESERVED       |              |              |                          |                   |                  |
| R-0h                  | R-0h                    | R-0h           |              |              |                          |                   |                  |
| 7                     | 6                       | 5              | 4            | 3            | 2                        | 1                 | 0                |
| RESERVED              |                         |                |              |              | RESERVED                 | RESERVED          | RESERVED         |
| R-0h                  |                         |                |              |              | R-0h                     | R-0h              | R-0h             |

**表 7-48. CONTROLLER\_FAULT\_STATUS Register Field Descriptions**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 31  | CONTROLLER_FAULT | R    | 0h    | Logic OR of controller fault status registers<br>0h = No controller fault condition is detected<br>1h = Controller fault condition is detected |
| 30  | RESERVED         | R    | 0h    | Reserved   |
| 29  | IPD_FREQ_FAULT   | R    | 0h    | Indicates IPD frequency fault<br>0h = No IPD frequency fault detected<br>1h = IPD frequency fault detected                                     |
| 28  | IPD_T1_FAULT     | R    | 0h    | Indicates IPD T1 fault<br>0h = No IPD T1 fault detected<br>1h = IPD T1 fault detected  |

**表 7-48. CONTROLLER\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit  | Field                    | Type | Reset | Description   |
|------|--------------------------|------|-------|---|
| 27   | IPD_T2_FAULT             | R    | 0h    | Indicates IPD T2 fault<br>0h = No IPD T2 fault detected<br>1h = IPD T2 fault detected   |
| 26   | BUS_CURRENT_LIMIT_STATUS | R    | 0h    | Indicates status of bus current limit<br>0h = No bus current limit fault detected<br>1h = Bus current limit fault detected                    |
| 25   | MPET_IPD_FAULT           | R    | 0h    | Indicates error during resistance and inductance measurement<br>0h = No MPET IPD fault detected<br>1h = MPET IPD fault detected               |
| 24   | MPET_BEMF_FAULT          | R    | 0h    | Indicates error during BEMF constant measurement<br>0h = No MPET BEMF fault detected<br>1h = MPET BEMF fault detected                         |
| 23   | ABN_SPEED                | R    | 0h    | Indicates abnormal speed motor lock condition<br>0h = No abnormal speed fault detected<br>1h = Abnormal speed fault detected                  |
| 22   | ABN_BEMF                 | R    | 0h    | Indicates abnormal BEMF motor lock condition<br>0h = No abnormal BEMF fault detected<br>1h = Abnormal BEMF fault detected                     |
| 21   | NO_MTR                   | R    | 0h    | Indicates no motor fault<br>0h = No motor fault not detected<br>1h = No motor fault detected  |
| 20   | MTR_LCK                  | R    | 0h    | Indicates when one of the motor lock is triggered<br>0h = Motor lock fault not detected<br>1h = Motor lock fault detected                     |
| 19   | LOCK_ILIMIT              | R    | 0h    | Indicates lock Ilimit fault<br>0h = No lock current limit fault detected<br>1h = Lock current limit fault detected                            |
| 18   | HW_LOCK_ILIMIT           | R    | 0h    | Indicates hardware lock Ilimit fault<br>0h = No hardware lock current limit fault detected<br>1h = Hardware lock current limit fault detected |
| 17   | MTR_UNDER_VOLTAGE        | R    | 0h    | Indicates motor undervoltage fault<br>0h = No motor undervoltage detected<br>1h = Motor undervoltage detected                                 |
| 16   | MTR_OVER_VOLTAGE         | R    | 0h    | Indicates motor overvoltage fault<br>0h = No motor overvoltage detected<br>1h = Motor overvoltage detected                                    |
| 15   | SPEED_LOOP_SATURATION    | R    | 0h    | Indicates speed loop saturation<br>0h = No speed loop saturation detected<br>1h = Speed loop saturation detected                              |
| 14   | CURRENT_LOOP_SATURATION  | R    | 0h    | Indicates current loop saturation<br>0h = No current loop saturation detected<br>1h = Current loop saturation detected                        |
| 13-3 | RESERVED                 | R    | 0h    | Reserved  |
| 2    | RESERVED                 | R    | 0h    | Reserved  |
| 1    | RESERVED                 | R    | 0h    | Reserved  |
| 0    | RESERVED                 | R    | 0h    | Reserved  |

## 7.8.2 System\_Status Registers

[SYSTEM\\_STATUS Registers](#) lists the memory-mapped registers for the System\_Status registers. All register offset addresses not listed in [SYSTEM\\_STATUS Registers](#) should be considered as reserved locations and the register contents should not be modified.

**表 7-49. SYSTEM\_STATUS Registers**

| Address | Acronym          | Register Name          | Section                   |
|---------|------------------|------------------------|---------------------------|
| E4h     | ALGO_STATUS      | System Status Register | <a href="#">节 7.8.2.1</a> |
| E6h     | MTR_PARAMS       | System Status Register | <a href="#">节 7.8.2.2</a> |
| E8h     | ALGO_STATUS_MPET | System Status Register | <a href="#">节 7.8.2.3</a> |

Complex bit access types are encoded to fit into small table cells. [System\\_Status Access Type Codes](#) shows the codes that are used for access types in this section.

**表 7-50. System\_Status Access Type Codes**

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

### 7.8.2.1 ALGO\_STATUS Register (Address = E4h) [Reset = 0000000h]

ALGO\_STATUS is shown in [ALGO\\_STATUS Register](#) and described in [ALGO\\_STATUS Register Field Descriptions](#).

Return to the [SYSTEM\\_STATUS Registers](#).

Status of various system and algorithm parameters

**图 7-81. ALGO\_STATUS Register**

|          |    |    |    |          |          |          |          |
|----------|----|----|----|----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27       | 26       | 25       | 24       |
| VOLT_MAG |    |    |    |          |          |          |          |
| R-0h     |    |    |    |          |          |          |          |
| 23       | 22 | 21 | 20 | 19       | 18       | 17       | 16       |
| VOLT_MAG |    |    |    |          |          |          |          |
| R-0h     |    |    |    |          |          |          |          |
| 15       | 14 | 13 | 12 | 11       | 10       | 9        | 8        |
| RESERVED |    |    |    |          |          |          |          |
| R-0h     |    |    |    |          |          |          |          |
| 7        | 6  | 5  | 4  | 3        | 2        | 1        | 0        |
| RESERVED |    |    |    | RESERVED | RESERVED | RESERVED | RESERVED |
| R-0h     |    |    |    | R-0h     | R-0h     | R-0h     | R-0h     |

**表 7-51. ALGO\_STATUS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 31-16 | VOLT_MAG | R    | 0h    | 16-bit value indicating output voltage magnitude. Voltage magnitude = (VOLT_MAG * 100 / 32767) % |
| 15-4  | RESERVED | R    | 0h    | Reserved   |
| 3     | RESERVED | R    | 0h    | Reserved   |



表 7-51. ALGO\_STATUS Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 2   | RESERVED | R    | 0h    | Reserved    |
| 1   | RESERVED | R    | 0h    | Reserved    |
| 0   | RESERVED | R    | 0h    | Reserved    |

### 7.8.2.2 MTR\_PARAMS Register (Address = E6h) [Reset = 0000000h]

MTR\_PARAMS is shown in [MTR\\_PARAMS Register](#) and described in [MTR\\_PARAMS Register Field Descriptions](#).

Return to the [SYSTEM\\_STATUS Registers](#).

Status of various motor parameters

图 7-82. MTR\_PARAMS Register

|         |    |    |    |    |    |    |    |                  |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MOTOR_R |    |    |    |    |    |    |    | MOTOR_BEMF_CONST |    |    |    |    |    |    |    |
| R-0h    |    |    |    |    |    |    |    | R-0h             |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MOTOR_L |    |    |    |    |    |    |    | RESERVED         |    |    |    |    |    |    |    |
| R-0h    |    |    |    |    |    |    |    | R-0h             |    |    |    |    |    |    |    |

表 7-52. MTR\_PARAMS Register Field Descriptions

| Bit   | Field            | Type | Reset | Description                                      |
|-------|------------------|------|-------|--|
| 31-24 | MOTOR_R          | R    | 0h    | 8-bit value indicating measured motor resistance |
| 23-16 | MOTOR_BEMF_CONST | R    | 0h    | 8-bit value indicating measured BEMF constant    |
| 15-8  | MOTOR_L          | R    | 0h    | 8-bit value indicating measured motor inductance |
| 7-0   | RESERVED         | R    | 0h    | Reserved   |

### 7.8.2.3 ALGO\_STATUS\_MPET Register (Address = E8h) [Reset = 0000000h]

ALGO\_STATUS\_MPET is shown in [ALGO\\_STATUS\\_MPET Register](#) and described in [ALGO\\_STATUS\\_MPET Register Field Descriptions](#).

Return to the [SYSTEM\\_STATUS Registers](#).

Status of various MPET parameters

图 7-83. ALGO\_STATUS\_MPET Register

|                   |                   |                    |                      |               |    |    |    |
|-------------------|-------------------|--------------------|----------------------|---------------|----|----|----|
| 31                | 30                | 29                 | 28                   | 27            | 26 | 25 | 24 |
| MPET_R_STAT<br>US | MPET_L_STAT<br>US | MPET_KE_STA<br>TUS | MPET_MECH_<br>STATUS | MPET_PWM_FREQ |    |    |    |
| R-0h              | R-0h              | R-0h               | R-0h                 | R-0h          |    |    |    |
| 23                | 22                | 21                 | 20                   | 19            | 18 | 17 | 16 |
| RESERVED          |                   |                    |                      |               |    |    |    |
| R-0h              |                   |                    |                      |               |    |    |    |
| 15                | 14                | 13                 | 12                   | 11            | 10 | 9  | 8  |
| RESERVED          |                   |                    |                      |               |    |    |    |
| R-0h              |                   |                    |                      |               |    |    |    |
| 7                 | 6                 | 5                  | 4                    | 3             | 2  | 1  | 0  |
| RESERVED          |                   |                    |                      |               |    |    |    |

图 7-83. ALGO\_STATUS\_MPET Register (continued)

R-0h

表 7-53. ALGO\_STATUS\_MPET Register Field Descriptions

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 31    | MPET_R_STATUS    | R    | 0h    | Indicates status of resistance measurement  |
| 30    | MPET_L_STATUS    | R    | 0h    | Indicates status of inductance measurement  |
| 29    | MPET_KE_STATUS   | R    | 0h    | Indicates status of BEMF constant measurement   |
| 28    | MPET_MECH_STATUS | R    | 0h    | Indicates status of mechanical parameter measurement  |
| 27-24 | MPET_PWM_FREQ    | R    | 0h    | 4-bit value indicating MPET recommended PWM switching frequency based on electrical time constant |
| 23-0  | RESERVED         | R    | 0h    | Reserved  |

### 7.8.3 Device\_Control Registers

[DEVICE\\_CONTROL Registers](#) lists the memory-mapped registers for the Device\_Control registers. All register offset addresses not listed in [DEVICE\\_CONTROL Registers](#) should be considered as reserved locations and the register contents should not be modified.

表 7-54. DEVICE\_CONTROL Registers

| Address | Acronym  | Register Name | Section   |
|---------|----------|---------------|-----------|
| EAh     | DEV_CTRL |               | 节 7.8.3.1 |

Complex bit access types are encoded to fit into small table cells. [Device\\_Control Access Type Codes](#) shows the codes that are used for access types in this section.

表 7-55. Device\_Control Access Type Codes

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Write Type</b>             |      |  |
| W                             | W    | Write                                  |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

#### 7.8.3.1 DEV\_CTRL Register (Address = EAh) [Reset = 0000000h]

DEV\_CTRL is shown in [DEV\\_CTRL Register](#) and described in [DEV\\_CTRL Register Field Descriptions](#).

Return to the [DEVICE\\_CONTROL Registers](#).

图 7-84. DEV\_CTRL Register

| 31                      | 30          | 29      | 28                  | 27                      | 26              | 25       | 24 |
|-------------------------|-------------|---------|---------------------|-------------------------|-----------------|----------|----|
| EEPROM_WRT              | EEPROM_READ | CLR_FLT | CLR_FLT_RETRY_COUNT | EEPROM_WRITE_ACCESS_KEY |                 |          |    |
| R/W-0h                  | R/W-0h      | W-0h    | W-0h                | W-0h                    |                 |          |    |
| 23                      | 22          | 21      | 20                  | 19                      | 18              | 17       | 16 |
| EEPROM_WRITE_ACCESS_KEY |             |         |                     | FORCED_ALIGN_ANGLE      |                 |          |    |
| W-0h                    |             |         |                     | W-0h                    |                 |          |    |
| 15                      | 14          | 13      | 12                  | 11                      | 10              | 9        | 8  |
| FORCED_ALIGN_ANGLE      |             |         |                     |                         | WATCHDOG_TICKLE | RESERVED |    |

图 7-84. DEV\_CTRL Register (continued)

|          |   |        |   |   |      |   |   |
|----------|---|--------|---|---|------|---|---|
| W-0h     |   | R/W-0h |   |   | W-0h |   |   |
| 7        | 6 | 5      | 4 | 3 | 2    | 1 | 0 |
| RESERVED |   |        |   |   |      |   |   |
| W-0h     |   |        |   |   |      |   |   |

表 7-56. DEV\_CTRL Register Field Descriptions

| Bit   | Field                   | Type | Reset | Description  |
|-------|-------------------------|------|-------|--|
| 31    | EEPROM_WRT              | R/W  | 0h    | Write the configuration to EEPROM  |
| 30    | EEPROM_READ             | R/W  | 0h    | Read the default configuration from EEPROM   |
| 29    | CLR_FLT                 | W    | 0h    | Clears all faults  |
| 28    | CLR_FLT_RETRY_COUNT     | W    | 0h    | Clears fault retry count   |
| 27-20 | EEPROM_WRITE_ACCESS_KEY | W    | 0h    | EEPROM write access key  |
| 19-11 | FORCED_ALIGN_ANGLE      | W    | 0h    | 9-bit value (in °) used during forced align state ( FORCE_ALIGN_EN = 1) Angle applied (°) = FORCED_ALIGN_ANGLE % 360°                                    |
| 10    | WATCHDOG_TICKLE         | R/W  | 0h    | RAM bit to tickle watchdog in I2C mode. This bit should be written to 1b by external controller every EXT_WD_CONFIG. MCF8316A will reset this bit to 0b. |
| 9-0   | RESERVED                | W    | 0h    | Reserved   |

## 7.8.4 Algorithm\_Control Registers

[ALGORITHM\\_CONTROL Registers](#) lists the memory-mapped registers for the Algorithm\_Control registers. All register offset addresses not listed in [ALGORITHM\\_CONTROL Registers](#) should be considered as reserved locations and the register contents should not be modified.

表 7-57. ALGORITHM\_CONTROL Registers

| Address | Acronym    | Register Name                  | Section                   |
|---------|------------|--------------------------------|---------------------------|
| ECh     | ALGO_CTRL1 | Algorithm Control Register     | <a href="#">节 7.8.4.1</a> |
| EEh     | ALGO_CTRL2 | Algorithm Control Register     | <a href="#">节 7.8.4.2</a> |
| F0h     | CURRENT_PI | Current PI Controller Register | <a href="#">节 7.8.4.3</a> |
| F2h     | SPEED_PI   | Speed PI Controller Register   | <a href="#">节 7.8.4.4</a> |

Complex bit access types are encoded to fit into small table cells. [Algorithm\\_Control Access Type Codes](#) shows the codes that are used for access types in this section.

表 7-58. Algorithm\_Control Access Type Codes

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Write Type</b>             |      |  |
| W                             | W    | Write                                  |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

### 7.8.4.1 ALGO\_CTRL1 Register (Address = ECh) [Reset = 0000000h]

ALGO\_CTRL1 is shown in [ALGO\\_CTRL1 Register](#) and described in [ALGO\\_CTRL1 Register Field Descriptions](#). Return to the [ALGORITHM\\_CONTROL Registers](#).

Algorithm control register for debug

图 7-85. ALGO\_CTRL1 Register

|                             |                |                           |              |              |                           |                             |    |
|-----------------------------|----------------|---------------------------|--------------|--------------|---------------------------|-----------------------------|----|
| 31                          | 30             | 29                        | 28           | 27           | 26                        | 25                          | 24 |
| OVERRIDE                    |                | DIGITAL_SPEED_CTRL        |              |              |                           |                             |    |
| W-0h                        |                | W-0h                      |              |              |                           |                             |    |
| 23                          | 22             | 21                        | 20           | 19           | 18                        | 17                          | 16 |
| DIGITAL_SPEED_CTRL          |                |                           |              |              |                           |                             |    |
| W-0h                        |                |                           |              |              |                           |                             |    |
| 15                          | 14             | 13                        | 12           | 11           | 10                        | 9                           | 8  |
| CLOSED_LOOP_DIS             | FORCE_ALIGN_EN | FORCE_SLOW_FIRST_CYCLE_EN | FORCE_IPD_EN | FORCE_ISD_EN | FORCE_ALIGN_ANGLE_SRC_SEL | FORCE_IQ_REF_SPEED_LOOP_DIS |    |
| W-0h                        | W-0h           | W-0h                      | W-0h         | W-0h         | W-0h                      | W-0h                        |    |
| 7                           | 6              | 5                         | 4            | 3            | 2                         | 1                           | 0  |
| FORCE_IQ_REF_SPEED_LOOP_DIS |                |                           |              |              |                           |                             |    |
| W-0h                        |                |                           |              |              |                           |                             |    |

表 7-59. ALGO\_CTRL1 Register Field Descriptions

| Bit   | Field                     | Type | Reset | Description  |
|-------|---------------------------|------|-------|--|
| 31    | OVERRIDE                  | W    | 0h    | Use to control the SPD_CTRL bits. If OVERRIDE = 1b, speed command can be written by the user through serial interface.<br>0h = SPEED_CMD using Analog/PWM/Freq mode<br>1h = SPEED_CMD using SPD_CTRL[14:0]   |
| 30-16 | DIGITAL_SPEED_CTRL        | W    | 0h    | Digital speed control. If OVERRIDE = 1b, then SPEED_CMD is control using DIGITAL_SPEED_CTRL  |
| 15    | CLOSED_LOOP_DIS           | W    | 0h    | Use to disable closed loop<br>0h = Enable Closed Loop<br>1h = Disable Closed loop, motor commutation in open loop  |
| 14    | FORCE_ALIGN_EN            | W    | 0h    | Force align state enable<br>0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN<br>1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN  |
| 13    | FORCE_SLOW_FIRST_CYCLE_EN | W    | 0h    | Force slow first cycle enable<br>0h = Disable Force Slow First Cycle state, device comes out of slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE<br>1h = Enable Force Slow First Cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE |
| 12    | FORCE_IPD_EN              | W    | 0h    | Force IPD enable<br>0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD<br>1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD  |
| 11    | FORCE_ISD_EN              | W    | 0h    | Force ISD enable<br>0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set<br>1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set  |

表 7-59. ALGO\_CTRL1 Register Field Descriptions (continued)

| Bit | Field                       | Type | Reset | Description  |
|-----|-----------------------------|------|-------|--|
| 10  | FORCE_ALIGN_ANGLE_SRC_SEL   | W    | 0h    | Force align angle state source select<br>0h = Force Align Angle defined by ALIGN_ANGLE<br>1h = Force Align Angle defined by FORCED_ALIGN_ANGLE   |
| 9-0 | FORCE_IQ_REF_SPEED_LOOP_DIS | W    | 0h    | Sets Iq_ref when speed loop is disabled If SPEED_LOOP_DIS = 1b, then Iq_ref is set using IQ_REF_SPEED_LOOP_DIS<br>$Iq\_ref = (FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS / 500) * 10$ , if $FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS < 500$ -<br>$(FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS - 512) / 500 * 10$ if $FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS > 512$ Valid values are 0 to 500 and 512 to 1000 |

#### 7.8.4.2 ALGO\_CTRL2 Register (Address = EEh) [Reset = 0000000h]

ALGO\_CTRL2 is shown in [ALGO\\_CTRL2 Register](#) and described in [ALGO\\_CTRL2 Register Field Descriptions](#).  
Return to the [ALGORITHM\\_CONTROL Registers](#).

Algorithm control register for debug

图 7-86. ALGO\_CTRL2 Register

|                           |          |        |        |         |                  |                           |      |
|---------------------------|----------|--------|--------|---------|------------------|---------------------------|------|
| 31                        | 30       | 29     | 28     | 27      | 26               | 25                        | 24   |
| RESERVED                  |          |        |        |         | CURRENT_LOOP_DIS | FORCE_VD_CURRENT_LOOP_DIS |      |
| W-0h                      |          |        |        |         | W-0h             | W-0h                      |      |
| 23                        | 22       | 21     | 20     | 19      | 18               | 17                        | 16   |
| FORCE_VD_CURRENT_LOOP_DIS |          |        |        |         |                  |                           |      |
| W-0h                      |          |        |        |         |                  |                           |      |
| 15                        | 14       | 13     | 12     | 11      | 10               | 9                         | 8    |
| FORCE_VQ_CURRENT_LOOP_DIS |          |        |        |         |                  |                           |      |
| W-0h                      |          |        |        |         |                  |                           |      |
| 7                         | 6        | 5      | 4      | 3       | 2                | 1                         | 0    |
| FORCE_VQ_CURRENT_LOOP_DIS | MPET_CMD | MPET_R | MPET_L | MPET_KE | MPET_MECH        | MPET_WRITE_SHADOW         |      |
| W-0h                      | W-0h     | W-0h   | W-0h   | W-0h    | W-0h             | W-0h                      | W-0h |

表 7-60. ALGO\_CTRL2 Register Field Descriptions

| Bit   | Field                     | Type | Reset | Description  |
|-------|---------------------------|------|-------|--|
| 31-27 | RESERVED                  | W    | 0h    | Reserved   |
| 26    | CURRENT_LOOP_DIS          | W    | 0h    | Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = 1b, current loop and speed loop are disabled<br>0h = Enable Current Loop<br>1h = Disable Current Loop  |
| 25-16 | FORCE_VD_CURRENT_LOOP_DIS | W    | 0h    | Sets Vd_ref when current loop and speed loop are disabled If CURRENT_LOOP_DIS = 1b, then Vd is controlled using FORCE_VD_CURRENT_LOOP_DIS<br>$Vd\_ref = (FORCE\_VD\_CURRENT\_LOOP\_DIS / 500)$ if $FORCE\_VD\_CURRENT\_LOOP\_DIS < 500$ -<br>$(FORCE\_VD\_CURRENT\_LOOP\_DIS - 512) / 500$ if $FORCE\_VD\_CURRENT\_LOOP\_DIS > 512$ Valid values: 0 to 500 and 512 to 1000 |

表 7-60. ALGO\_CTRL2 Register Field Descriptions (continued)

| Bit  | Field                     | Type | Reset | Description   |
|------|---------------------------|------|-------|---|
| 15-6 | FORCE_VQ_CURRENT_LOOP_DIS | W    | 0h    | Sets Vq_ref when current loop speed loop are disabled. If CURRENT_LOOP_DIS = 1b, then Vq is controlled using FORCE_VQ_CURRENT_LOOP_DIS. $Vq\_ref = (FORCE\_VQ\_CURRENT\_LOOP\_DIS / 500)$ if $FORCE\_VQ\_CURRENT\_LOOP\_DIS < 500$ - $(FORCE\_VQ\_CURRENT\_LOOP\_DIS - 512) / 500$ if $FORCE\_VQ\_CURRENT\_LOOP\_DIS > 512$ . Valid values: 0 to 500 and 512 to 1000. |
| 5    | MPET_CMD                  | W    | 0h    | Initiates motor parameter measurement routine when set to 1b.   |
| 4    | MPET_R                    | W    | 0h    | Enables motor resistance measurement during motor parameter measurement routine.<br>0h = Disable Motor Resistance measurement during motor parameter measurement routine<br>1h = Enable Motor Resistance measurement during motor parameter measurement routine.  |
| 3    | MPET_L                    | W    | 0h    | Enables motor inductance measurement during motor parameter measurement routine.<br>0h = Disable Motor Inductance measurement during motor parameter measurement routine<br>1h = Enable Motor Inductance measurement during motor parameter measurement routine.  |
| 2    | MPET_KE                   | W    | 0h    | Enables motor BEMF constant measurement during motor parameter measurement routine.<br>0h = Disables Motor BEMF constant measurement during motor parameter measurement routine<br>1h = Enable Motor BEMF constant measurement during motor parameter measurement routine.  |
| 1    | MPET_MECH                 | W    | 0h    | Enables motor mechanical parameter measurement during motor parameter measurement routine.<br>0h = Disable Motor mechanical parameter measurement during motor parameter measurement routine<br>1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine.  |
| 0    | MPET_WRITE_SHADOW         | W    | 0h    | Write measured parameters to shadow register when set to 1b.  |

### 7.8.4.3 CURRENT\_PI Register (Address = F0h) [Reset = 0000000h]

CURRENT\_PI is shown in [CURRENT\\_PI Register](#) and described in [CURRENT\\_PI Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONTROL Registers](#).

Current PI controller used

图 7-87. CURRENT\_PI Register

|                 |    |    |    |    |          |    |    |    |    |                 |    |    |    |    |    |
|-----------------|----|----|----|----|----------|----|----|----|----|-----------------|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21              | 20 | 19 | 18 | 17 | 16 |
| CURRENT_LOOP_KP |    |    |    |    |          |    |    |    |    | CURRENT_LOOP_KI |    |    |    |    |    |
| R-0h            |    |    |    |    |          |    |    |    |    | R-0h            |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5               | 4  | 3  | 2  | 1  | 0  |
| CURRENT_LOOP_KI |    |    |    |    | RESERVED |    |    |    |    |                 |    |    |    |    |    |
| R-0h            |    |    |    |    | R-0h     |    |    |    |    |                 |    |    |    |    |    |

表 7-61. CURRENT\_PI Register Field Descriptions

| Bit   | Field           | Type | Reset | Description  |
|-------|-----------------|------|-------|--|
| 31-22 | CURRENT_LOOP_KP | R    | 0h    | 10-bit value for current loop Kp; same scaling as CURR_LOOP_KP |
| 21-12 | CURRENT_LOOP_KI | R    | 0h    | 10-bit value for current loop Ki; same scaling as CURR_LOOP_KI |
| 11-0  | RESERVED        | R    | 0h    | Reserved   |

#### 7.8.4.4 SPEED\_PI Register (Address = F2h) [Reset = 0000000h]

SPEED\_PI is shown in [SPEED\\_PI Register](#) and described in [SPEED\\_PI Register Field Descriptions](#).

Return to the [ALGORITHM\\_CONTROL Registers](#).

Speed PI controller used

图 7-88. SPEED\_PI Register

|               |    |    |    |          |    |    |    |    |    |               |    |    |    |    |    |
|---------------|----|----|----|----------|----|----|----|----|----|---------------|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27       | 26 | 25 | 24 | 23 | 22 | 21            | 20 | 19 | 18 | 17 | 16 |
| SPEED_LOOP_KP |    |    |    |          |    |    |    |    |    | SPEED_LOOP_KI |    |    |    |    |    |
| R-0h          |    |    |    |          |    |    |    |    |    | R-0h          |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11       | 10 | 9  | 8  | 7  | 6  | 5             | 4  | 3  | 2  | 1  | 0  |
| SPEED_LOOP_KI |    |    |    | RESERVED |    |    |    |    |    |               |    |    |    |    |    |
| R-0h          |    |    |    | R-0h     |    |    |    |    |    |               |    |    |    |    |    |

表 7-62. SPEED\_PI Register Field Descriptions

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---|
| 31-22 | SPEED_LOOP_KP | R    | 0h    | 10-bit value for speed loo Kp; same scaling as SPD_LOOP_KP  |
| 21-12 | SPEED_LOOP_KI | R    | 0h    | 10-bit value for speed loop Ki; same scaling as SPD_LOOP_KI |
| 11-0  | RESERVED      | R    | 0h    | Reserved  |

#### 7.8.5 Algorithm\_Variables Registers

[ALGORITHM\\_VARIABLES Registers](#) lists the memory-mapped registers for the Algorithm\_Variables registers. All register offset addresses not listed in [ALGORITHM\\_VARIABLES Registers](#) should be considered as reserved locations and the register contents should not be modified.

表 7-63. ALGORITHM\_VARIABLES Registers

| Address | Acronym               | Register Name                        | Section                    |
|---------|-----------------------|--------------------------------------|----------------------------|
| 210h    | ALGORITHM_STATE       | Current Algorithm State Register     | <a href="#">节 7.8.5.1</a>  |
| 216h    | FG_SPEED_FDBK         | FG Speed Feedback Register           | <a href="#">节 7.8.5.2</a>  |
| 410h    | BUS_CURRENT           | Calculated DC Bus Current Register   | <a href="#">节 7.8.5.3</a>  |
| 43Eh    | PHASE_CURRENT_A       | Measured Current on Phase A Register | <a href="#">节 7.8.5.4</a>  |
| 440h    | PHASE_CURRENT_B       | Measured Current on Phase B Register | <a href="#">节 7.8.5.5</a>  |
| 442h    | PHASE_CURRENT_C       | Measured Current on Phase C Register | <a href="#">节 7.8.5.6</a>  |
| 466h    | CSA_GAIN_FEEDBACK     | CSA Gain Register                    | <a href="#">节 7.8.5.7</a>  |
| 476h    | VOLTAGE_GAIN_FEEDBACK | Voltage Gain Register                | <a href="#">节 7.8.5.8</a>  |
| 478h    | VM_VOLTAGE            | VM Voltage Register                  | <a href="#">节 7.8.5.9</a>  |
| 47Eh    | PHASE_VOLTAGE_VA      | Phase Voltage Register               | <a href="#">节 7.8.5.10</a> |
| 480h    | PHASE_VOLTAGE_VB      | Phase Voltage Register               | <a href="#">节 7.8.5.11</a> |
| 482h    | PHASE_VOLTAGE_VC      | Phase Voltage Register               | <a href="#">节 7.8.5.12</a> |
| 4BAh    | SIN_COMMUTATION_ANGLE | Sine of Commutation Angle            | <a href="#">节 7.8.5.13</a> |
| 4BCh    | COS_COMMUTATION_ANGLE | Cosine of Commutation Angle          | <a href="#">节 7.8.5.14</a> |
| 4D4h    | IALPHA                | IALPHA Current Register              | <a href="#">节 7.8.5.15</a> |

表 7-63. ALGORITHM\_VARIABLES Registers (continued)

| Address | Acronym               | Register Name                       | Section    |
|---------|-----------------------|-------------------------------------|------------|
| 4D6h    | IBETA                 | IBETA Current Register              | 节 7.8.5.16 |
| 4D8h    | VALPHA                | VALPHA Voltage Register             | 节 7.8.5.17 |
| 4DAh    | VBETA                 | VBETA Voltage Register              | 节 7.8.5.18 |
| 4E4h    | ID                    | Measured d-axis Current Register    | 节 7.8.5.19 |
| 4E6h    | IQ                    | Measured q-axis Current Register    | 节 7.8.5.20 |
| 4E8h    | VD                    | VD Voltage Register                 | 节 7.8.5.21 |
| 4EAh    | VQ                    | VQ Voltage Register                 | 节 7.8.5.22 |
| 524h    | IQ_REF_ROTATOR_ALIGN  | Align Current Reference             | 节 7.8.5.23 |
| 53Ah    | SPEED_REF_OPEN_LOOP   | Open Loop Speed Register            | 节 7.8.5.24 |
| 548h    | IQ_REF_OPEN_LOOP      | Open Loop Current Reference         | 节 7.8.5.25 |
| 5CCh    | SPEED_REF_CLOSED_LOOP | Speed Reference Register            | 节 7.8.5.26 |
| 5FCh    | ID_REF_CLOSED_LOOP    | Reference for Current Loop Register | 节 7.8.5.27 |
| 5FEh    | IQ_REF_CLOSED_LOOP    | Reference for Current Loop Register | 节 7.8.5.28 |
| 67Ah    | ISD_STATE             | ISD State Register                  | 节 7.8.5.29 |
| 684h    | ISD_SPEED             | ISD Speed Register                  | 节 7.8.5.30 |
| 6B8h    | IPD_STATE             | IPD State Register                  | 节 7.8.5.31 |
| 6FCh    | IPD_ANGLE             | Calculated IPD Angle Register       | 节 7.8.5.32 |
| 742h    | ED                    | Estimated BEMF EQ Register          | 节 7.8.5.33 |
| 744h    | EQ                    | Estimated BEMF ED Register          | 节 7.8.5.34 |
| 752h    | SPEED_FDBK            | Speed Feedback Register             | 节 7.8.5.35 |
| 756h    | THETA_EST             | Estimated Motor Position Register   | 节 7.8.5.36 |

Complex bit access types are encoded to fit into small table cells. [Algorithm\\_Variables Access Type Codes](#) shows the codes that are used for access types in this section.

表 7-64. Algorithm\_Variables Access Type Codes

| Access Type                   | Code | Description                            |
|-------------------------------|------|--|
| <b>Read Type</b>              |      |  |
| R                             | R    | Read                                   |
| <b>Reset or Default Value</b> |      |  |
| -n                            |      | Value after reset or the default value |

### 7.8.5.1 ALGORITHM\_STATE Register (Address = 210h) [Reset = 0000000h]

ALGORITHM\_STATE is shown in [ALGORITHM\\_STATE Register](#) and described in [ALGORITHM\\_STATE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Current Algorithm State Register

图 7-89. ALGORITHM\_STATE Register

| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ALGORITHM_STATE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0h            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |



表 7-65. ALGORITHM\_STATE Register Field Descriptions

| Bit   | Field           | Type | Reset | Description  |
|-------|-----------------|------|-------|--|
| 31-16 | RESERVED        | R    | 0h    | Reserved   |
| 15-0  | ALGORITHM_STATE | R    | 0h    | 16-bit value indicating current state of device<br>0h = MOTOR_IDLE<br>1h = MOTOR_ISD<br>2h = MOTOR_TRISTATE<br>3h = MOTOR_BRAKE_ON_START<br>4h = MOTOR_IPD<br>5h = MOTOR_SLOW_FIRST_CYCLE<br>6h = MOTOR_ALIGN<br>7h = MOTOR_OPEN_LOOP<br>8h = MOTOR_CLOSED_LOOP_UNALIGNED<br>9h = MOTOR_CLOSED_LOOP_ALIGNED<br>Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING<br>Bh = MOTOR_SOFT_STOP<br>Ch = MOTOR_RECIRCULATE_STOP<br>Dh = MOTOR_BRAKE_ON_STOP<br>Eh = MOTOR_FAULT<br>Fh = MOTOR_MPET_MOTOR_STOP_CHECK<br>10h = MOTOR_MPET_MOTOR_STOP_WAIT<br>11h = MOTOR_MPET_MOTOR_BRAKE<br>12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT<br>13h = MOTOR_MPET_RL_MEASURE<br>14h = MOTOR_MPET_KE_MEASURE<br>15h = MOTOR_MPET_STALL_CURRENT_MEASURE<br>16h = MOTOR_MPET_TORQUE_MODE<br>17h = MOTOR_MPET_DONE<br>18h = MOTOR_MPET_FAULT |

### 7.8.5.2 FG\_SPEED\_FDBK Register (Address = 216h) [Reset = 0000000h]

FG\_SPEED\_FDBK is shown in [FG\\_SPEED\\_FDBK Register](#) and described in [FG\\_SPEED\\_FDBK Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Speed Feedback from FG

图 7-90. FG\_SPEED\_FDBK Register

|               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FG_SPEED_FDBK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-66. FG\_SPEED\_FDBK Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 31-0 | FG_SPEED_FDBK | R    | 0h    | 32-bit value indicating FG estimated rotor speed; $FG_{EstimatedSpeed} (Hz) = (FG\_SPEED\_FDBK / 2^{27}) * MAX\_SPEED$ |

### 7.8.5.3 BUS\_CURRENT Register (Address = 410h) [Reset = 0000000h]

BUS\_CURRENT is shown in [BUS\\_CURRENT Register](#) and described in [BUS\\_CURRENT Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

## Calculated Supply Current Register

图 7-91. BUS\_CURRENT Register

|             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUS_CURRENT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-67. BUS\_CURRENT Register Field Descriptions

| Bit  | Field       | Type | Reset | Description  |
|------|-------------|------|-------|--|
| 31-0 | BUS_CURRENT | R    | 0h    | 32-bit value indicating DC bus current; $I_{dcBus} (A) = (BUS\_CURRENT / 2^{27}) * 1.25$ |

## 7.8.5.4 PHASE\_CURRENT\_A Register (Address = 43Eh) [Reset = 00000000h]

PHASE\_CURRENT\_A is shown in [PHASE\\_CURRENT\\_A Register](#) and described in [PHASE\\_CURRENT\\_A Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Measured current on Phase A Register

图 7-92. PHASE\_CURRENT\_A Register

|                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_CURRENT_A |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-68. PHASE\_CURRENT\_A Register Field Descriptions

| Bit  | Field           | Type | Reset | Description  |
|------|-----------------|------|-------|--|
| 31-0 | PHASE_CURRENT_A | R    | 0h    | 32-bit value indicating measured current on Phase A; $I_a (A) = (PHASE\_CURRENT\_A / 2^{27}) * 1.25$ |

## 7.8.5.5 PHASE\_CURRENT\_B Register (Address = 440h) [Reset = 00000000h]

PHASE\_CURRENT\_B is shown in [PHASE\\_CURRENT\\_B Register](#) and described in [PHASE\\_CURRENT\\_B Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Measured current on Phase B Register

图 7-93. PHASE\_CURRENT\_B Register

|                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_CURRENT_B |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-69. PHASE\_CURRENT\_B Register Field Descriptions

| Bit  | Field           | Type | Reset | Description  |
|------|-----------------|------|-------|--|
| 31-0 | PHASE_CURRENT_B | R    | 0h    | 32-bit value indicating measured current on Phase B; $I_b (A) = (PHASE\_CURRENT\_B / 2^{27}) * 1.25$ |

## 7.8.5.6 PHASE\_CURRENT\_C Register (Address = 442h) [Reset = 00000000h]

PHASE\_CURRENT\_C is shown in [PHASE\\_CURRENT\\_C Register](#) and described in [PHASE\\_CURRENT\\_C Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Measured current on Phase C Register

**图 7-94. PHASE\_CURRENT\_C Register**

|                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_CURRENT_C |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-70. PHASE\_CURRENT\_C Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description   |
|------|-----------------|------|-------|---|
| 31-0 | PHASE_CURRENT_C | R    | 0h    | 32-bit value indicating measured current on Phase C; $I_c$ (A) = $(\text{PHASE\_CURRENT\_C} / 2^{27}) * 1.25$ |

### 7.8.5.7 CSA\_GAIN\_FEEDBACK Register (Address = 466h) [Reset = 0000000h]

CSA\_GAIN\_FEEDBACK is shown in [CSA\\_GAIN\\_FEEDBACK Register](#) and described in [CSA\\_GAIN\\_FEEDBACK Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

VM Voltage Register

**图 7-95. CSA\_GAIN\_FEEDBACK Register**

|                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0h              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CSA_GAIN_FEEDBACK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0h              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**表 7-71. CSA\_GAIN\_FEEDBACK Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description   |
|-------|-------------------|------|-------|---|
| 31-16 | RESERVED          | R    | 0h    | Reserved  |
| 15-0  | CSA_GAIN_FEEDBACK | R    | 0h    | 16-bit value indicating current sense gain<br>0h = 1.2 V/A<br>1h = 0.6 V/A<br>2h = 0.3 V/A<br>3h = 0.15 V/A |

### 7.8.5.8 VOLTAGE\_GAIN\_FEEDBACK Register (Address = 476h) [Reset = 0000000h]

VOLTAGE\_GAIN\_FEEDBACK is shown in [VOLTAGE\\_GAIN\\_FEEDBACK Register](#) and described in [VOLTAGE\\_GAIN\\_FEEDBACK Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Voltage Gain Register

**图 7-96. VOLTAGE\_GAIN\_FEEDBACK Register**

|          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0h     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**图 7-96. VOLTAGE\_GAIN\_FEEDBACK Register (continued)**

|                       |
|-----------------------|
| VOLTAGE_GAIN_FEEDBACK |
| R-0h                  |

**表 7-72. VOLTAGE\_GAIN\_FEEDBACK Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description  |
|-------|-----------------------|------|-------|--|
| 31-16 | RESERVED              | R    | 0h    | Reserved   |
| 15-0  | VOLTAGE_GAIN_FEEDBACK | R    | 0h    | 16-bit value indicating voltage gain<br>0h = 60V<br>1h = 30V<br>2h = 15V |

**7.8.5.9 VM\_VOLTAGE Register (Address = 478h) [Reset = 0000000h]**

VM\_VOLTAGE is shown in [VM\\_VOLTAGE Register](#) and described in [VM\\_VOLTAGE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Supply voltage register

**图 7-97. VM\_VOLTAGE Register**

|   |
|---|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| VM_VOLTAGE  |
| R-0h  |

**表 7-73. VM\_VOLTAGE Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description  |
|------|------------|------|-------|--|
| 31-0 | VM_VOLTAGE | R    | 0h    | 32-bit value indicating DC bus voltage; DC Bus Voltage (V) = VM_VOLTAGE * 60 / 2 <sup>27</sup> |

**7.8.5.10 PHASE\_VOLTAGE\_VA Register (Address = 47Eh) [Reset = 0000000h]**

PHASE\_VOLTAGE\_VA is shown in [PHASE\\_VOLTAGE\\_VA Register](#) and described in [PHASE\\_VOLTAGE\\_VA Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Phase Voltage Register

**图 7-98. PHASE\_VOLTAGE\_VA Register**

|   |
|---|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| PHASE_VOLTAGE_VA  |
| R-0h  |

**表 7-74. PHASE\_VOLTAGE\_VA Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 31-0 | PHASE_VOLTAGE_VA | R    | 0h    | 32-bit value indicating phase voltage Va during ISD; Va (V) = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2 <sup>27</sup> ) |

**7.8.5.11 PHASE\_VOLTAGE\_VB Register (Address = 480h) [Reset = 0000000h]**

PHASE\_VOLTAGE\_VB is shown in [PHASE\\_VOLTAGE\\_VB Register](#) and described in [PHASE\\_VOLTAGE\\_VB Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Phase Voltage Register

图 7-99. PHASE\_VOLTAGE\_VB Register

|                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_VOLTAGE_VB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-75. PHASE\_VOLTAGE\_VB Register Field Descriptions

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 31-0 | PHASE_VOLTAGE_VB | R    | 0h    | 32-bit value indicating phase voltage Vb during ISD; $V_b (V) = \text{PHASE\_VOLTAGE\_VB} * 60 / (\text{sqrt}(3) * 2^{27})$ |

7.8.5.12 PHASE\_VOLTAGE\_VC Register (Address = 482h) [Reset = 0000000h]

PHASE\_VOLTAGE\_VC is shown in [PHASE\\_VOLTAGE\\_VC Register](#) and described in [PHASE\\_VOLTAGE\\_VC Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Phase Voltage Register

图 7-100. PHASE\_VOLTAGE\_VC Register

|                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_VOLTAGE_VC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-76. PHASE\_VOLTAGE\_VC Register Field Descriptions

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 31-0 | PHASE_VOLTAGE_VC | R    | 0h    | 32-bit value indicating phase voltage Vc during ISD; $V_c (V) = \text{PHASE\_VOLTAGE\_VC} * 60 / (\text{sqrt}(3) * 2^{27})$ |

7.8.5.13 SIN\_COMMUTATION\_ANGLE Register (Address = 4BAh) [Reset = 0000000h]

SIN\_COMMUTATION\_ANGLE is shown in [SIN\\_COMMUTATION\\_ANGLE Register](#) and described in [SIN\\_COMMUTATION\\_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Sine of Commutation Angle

图 7-101. SIN\_COMMUTATION\_ANGLE Register

|                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SIN_COMMUTATION_ANGLE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-77. SIN\_COMMUTATION\_ANGLE Register Field Descriptions

| Bit  | Field                 | Type | Reset | Description   |
|------|-----------------------|------|-------|---|
| 31-0 | SIN_COMMUTATION_ANGLE | R    | 0h    | 32-bit value indicating sine of commutation angle; $\text{sinCommutationAngle} = (\text{SIN\_COMMUTATION\_ANGLE} / 2^{27})$ |

7.8.5.14 COS\_COMMUTATION\_ANGLE Register (Address = 4BCh) [Reset = 0000000h]

COS\_COMMUTATION\_ANGLE is shown in [COS\\_COMMUTATION\\_ANGLE Register](#) and described in [COS\\_COMMUTATION\\_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Cosine of Commutation Angle

**图 7-102. COS\_COMMUTATION\_ANGLE Register**

|                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COS_COMMUTATION_ANGLE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-78. COS\_COMMUTATION\_ANGLE Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description   |
|------|-----------------------|------|-------|---|
| 31-0 | COS_COMMUTATION_ANGLE | R    | 0h    | 32-bit value indicating cosine of commutation angle; $\text{cosCommutationAngle} = (\text{COS\_COMMUTATION\_ANGLE} / 2^{27})$ |

### 7.8.5.15 IALPHA Register (Address = 4D4h) [Reset = 0000000h]

IALPHA is shown in [IALPHA Register](#) and described in [IALPHA Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

IALPHA Current Register

**图 7-103. IALPHA Register**

|        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IALPHA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-79. IALPHA Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description   |
|------|--------|------|-------|---|
| 31-0 | IALPHA | R    | 0h    | 32-bit value indicating calculated I_alpha; $I\_alpha(A) = (\text{IALPHA} / 2^{27}) * 1.25$ |

### 7.8.5.16 IBETA Register (Address = 4D6h) [Reset = 0000000h]

IBETA is shown in [IBETA Register](#) and described in [IBETA Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

IBETA Current Register

**图 7-104. IBETA Register**

|       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBETA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-80. IBETA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description  |
|------|-------|------|-------|--|
| 31-0 | IBETA | R    | 0h    | 32-bit value indicating calculated I_beta; $I\_beta(A) = (\text{IBETA} / 2^{27}) * 1.25$ |

### 7.8.5.17 VALPHA Register (Address = 4D8h) [Reset = 0000000h]

VALPHA is shown in [VALPHA Register](#) and described in [VALPHA Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

VALPHA Voltage Register

图 7-105. VALPHA Register

|        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VALPHA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-81. VALPHA Register Field Descriptions

| Bit  | Field  | Type | Reset | Description  |
|------|--------|------|-------|--|
| 31-0 | VALPHA | R    | 0h    | 32-bit value indicating calculated V_alpha; V_alpha (V) = (VALPHA / 2 <sup>27</sup> ) * 60 / sqrt(3) |

7.8.5.18 VBETA Register (Address = 4DAh) [Reset = 0000000h]

VBETA is shown in [VBETA Register](#) and described in [VBETA Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

VBETA Voltage Register

图 7-106. VBETA Register

|       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBETA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-82. VBETA Register Field Descriptions

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VBETA | R    | 0h    | 32-bit value indicating calculated V_beta; V_beta (V) = (VBETA / 2 <sup>27</sup> ) * 60 / sqrt(3) |

7.8.5.19 ID Register (Address = 4E4h) [Reset = 0000000h]

ID is shown in [ID Register](#) and described in [ID Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Measured d-axis Current Register

图 7-107. ID Register

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-83. ID Register Field Descriptions

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | ID    | R    | 0h    | 32-bit value indicating estimated Id; Id (A) = (ID / 2 <sup>27</sup> ) * 1.25 |

7.8.5.20 IQ Register (Address = 4E6h) [Reset = 0000000h]

IQ is shown in [IQ Register](#) and described in [IQ Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Measured q-axis Current Register

**图 7-108. IQ Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IQ   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-84. IQ Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | IQ    | R    | 0h    | 32-bit value indicating estimated Iq; Iq (A) = (IQ / 2 <sup>27</sup> ) * 1.25 |

**7.8.5.21 VD Register (Address = 4E8h) [Reset = 0000000h]**

VD is shown in [VD Register](#) and described in [VD Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

VD Voltage Register

**图 7-109. VD Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VD   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-85. VD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VD    | R    | 0h    | 32-bit value indicating applied Vd; Vd (V) = (VD / 2 <sup>27</sup> ) * 60 / sqrt(3) |

**7.8.5.22 VQ Register (Address = 4EAh) [Reset = 0000000h]**

VQ is shown in [VQ Register](#) and described in [VQ Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

VQ Voltage Register

**图 7-110. VQ Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VQ   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-86. VQ Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VQ    | R    | 0h    | 32-bit value indicating applied Vq; Vq (V) = (VQ / 2 <sup>27</sup> ) * 60 / sqrt(3) |

**7.8.5.23 IQ\_REF\_ROTOR\_ALIGN Register (Address = 524h) [Reset = 0000000h]**

IQ\_REF\_ROTOR\_ALIGN is shown in [IQ\\_REF\\_ROTOR\\_ALIGN Register](#) and described in [IQ\\_REF\\_ROTOR\\_ALIGN Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Align Current Reference

**图 7-111. IQ\_REF\_ROTOR\_ALIGN Register**

|                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IQ_REF_ROTOR_ALIGN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |



图 7-111. IQ\_REF\_ROTOR\_ALIGN Register (continued)

R-0h

表 7-87. IQ\_REF\_ROTOR\_ALIGN Register Field Descriptions

| Bit  | Field              | Type | Reset | Description   |
|------|--------------------|------|-------|---|
| 31-0 | IQ_REF_ROTOR_ALIGN | R    | 0h    | 32-bit value indicating Align Current Reference; IqRefRotorAlign (A) = (IQ_REF_ROTOR_ALIGN / 2 <sup>27</sup> ) * 1.25 |

#### 7.8.5.24 SPEED\_REF\_OPEN\_LOOP Register (Address = 53Ah) [Reset = 0000000h]

SPEED\_REF\_OPEN\_LOOP is shown in [SPEED\\_REF\\_OPEN\\_LOOP Register](#) and described in [SPEED\\_REF\\_OPEN\\_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Speed at which motor transitions to close loop

图 7-112. SPEED\_REF\_OPEN\_LOOP Register

| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| SPEED_REF_OPEN_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-88. SPEED\_REF\_OPEN\_LOOP Register Field Descriptions

| Bit  | Field               | Type | Reset | Description   |
|------|---------------------|------|-------|---|
| 31-0 | SPEED_REF_OPEN_LOOP | R    | 0h    | 32-bit value indicating open loop speed reference; OpenLoopSpeedRef (Hz) = (SPEED_REF_OPEN_LOOP / 2 <sup>27</sup> ) * MAX_SPEED |

#### 7.8.5.25 IQ\_REF\_OPEN\_LOOP Register (Address = 548h) [Reset = 0000000h]

IQ\_REF\_OPEN\_LOOP is shown in [IQ\\_REF\\_OPEN\\_LOOP Register](#) and described in [IQ\\_REF\\_OPEN\\_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Open Loop Current Reference

图 7-113. IQ\_REF\_OPEN\_LOOP Register

| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| IQ_REF_OPEN_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-89. IQ\_REF\_OPEN\_LOOP Register Field Descriptions

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 31-0 | IQ_REF_OPEN_LOOP | R    | 0h    | 32-bit value indicating Open Loop Current Reference IqRefOpenLoop (A) = (IQ_REF_OPEN_LOOP / 2 <sup>27</sup> ) * 1.25 |

#### 7.8.5.26 SPEED\_REF\_CLOSED\_LOOP Register (Address = 5CCh) [Reset = 0000000h]

SPEED\_REF\_CLOSED\_LOOP is shown in [SPEED\\_REF\\_CLOSED\\_LOOP Register](#) and described in [SPEED\\_REF\\_CLOSED\\_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Speed Reference Register

**图 7-114. SPEED\_REF\_CLOSED\_LOOP Register**

|                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPEED_REF_CLOSED_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-90. SPEED\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description  |
|------|-----------------------|------|-------|--|
| 31-0 | SPEED_REF_CLOSED_LOOP | R    | 0h    | 32-bit value indicating reference for speed loop; Speed reference in closed loop (Hz) = (SPEED_REF_CLOSED_LOOP / 2 <sup>27</sup> ) * MAX_SPEED |

**7.8.5.27 ID\_REF\_CLOSED\_LOOP Register (Address = 5FCh) [Reset = 0000000h]**

ID\_REF\_CLOSED\_LOOP is shown in [ID\\_REF\\_CLOSED\\_LOOP Register](#) and described in [ID\\_REF\\_CLOSED\\_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Reference for Current Loop Register

**图 7-115. ID\_REF\_CLOSED\_LOOP Register**

|                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID_REF_CLOSED_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-91. ID\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description  |
|------|--------------------|------|-------|--|
| 31-0 | ID_REF_CLOSED_LOOP | R    | 0h    | 32-bit value indicating Id_ref for flux loop; IdRefClosedLoop (A) = (ID_REF_CLOSED_LOOP / 2 <sup>27</sup> ) * 1.25 |

**7.8.5.28 IQ\_REF\_CLOSED\_LOOP Register (Address = 5FEh) [Reset = 0000000h]**

IQ\_REF\_CLOSED\_LOOP is shown in [IQ\\_REF\\_CLOSED\\_LOOP Register](#) and described in [IQ\\_REF\\_CLOSED\\_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Reference for Current Loop Register

**图 7-116. IQ\_REF\_CLOSED\_LOOP Register**

|                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IQ_REF_CLOSED_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-92. IQ\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description   |
|------|--------------------|------|-------|---|
| 31-0 | IQ_REF_CLOSED_LOOP | R    | 0h    | 32-bit value indicating Iq_ref for torque loop ; IqRefClosedLoop (A) = (IQ_REF_CLOSED_LOOP / 2 <sup>27</sup> ) * 1.25 |

**7.8.5.29 ISD\_STATE Register (Address = 67Ah) [Reset = 0000000h]**

ISD\_STATE is shown in [ISD\\_STATE Register](#) and described in [ISD\\_STATE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

ISD state Register

图 7-117. ISD\_STATE Register

|          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ISD_STATE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0h      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-93. ISD\_STATE Register Field Descriptions

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 31-16 | RESERVED  | R    | 0h    | Reserved   |
| 15-0  | ISD_STATE | R    | 0h    | 16-bit value indicating current ISD state<br>0h = ISD_INIT<br>1h = ISD_MOTOR_STOP_CHECK<br>2h = ISD_MOTOR_DIRECTION_CHECK<br>3h = ISD_COMPLETE<br>4h = ISD_FAULT |

### 7.8.5.30 ISD\_SPEED Register (Address = 684h) [Reset = 0000000h]

ISD\_SPEED is shown in [ISD\\_SPEED Register](#) and described in [ISD\\_SPEED Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

ISD Speed Register

图 7-118. ISD\_SPEED Register

|           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISD_SPEED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-94. ISD\_SPEED Register Field Descriptions

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--|
| 31-0 | ISD_SPEED | R    | 0h    | 32-bit value indicating calculated speed during ISD state; ISD_Speed (Hz) = (ISD_SPEED / 2 <sup>27</sup> ) * MAX_SPEED |

### 7.8.5.31 IPD\_STATE Register (Address = 6B8h) [Reset = 0000000h]

IPD\_STATE is shown in [IPD\\_STATE Register](#) and described in [IPD\\_STATE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

IPD state Register

图 7-119. IPD\_STATE Register

|          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IPD_STATE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0h      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-95. IPD\_STATE Register Field Descriptions

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-16 | RESERVED | R    | 0h    | Reserved    |

表 7-95. IPD\_STATE Register Field Descriptions (continued)

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--|
| 15-0 | IPD_STATE | R    | 0h    | 16-bit value indicating current IPD state<br>0h = IPD_INIT<br>1h = IPD_VECTOR_CONFIG<br>2h = IPD_RUN<br>3h = IPD_SLOW_RISE_CLOCK<br>4h = IPD_SLOW_FALL_CLOCK<br>5h = IPD_WAIT_CURRENT_DECAY<br>6h = IPD_GET_TIMES<br>7h = IPD_SET_NEXT_VECTOR<br>8h = IPD_CALC_SECTOR_RISE<br>9h = IPD_CALC_ROTOR_POSITION<br>Ah = IPD_CALC_ANGLE<br>Bh = IPD_COMPLETE<br>Ch = IPD_FAULT |

### 7.8.5.32 IPD\_ANGLE Register (Address = 6FCh) [Reset = 0000000h]

IPD\_ANGLE is shown in [IPD\\_ANGLE Register](#) and described in [IPD\\_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Calculated IPD Angle Register

图 7-120. IPD\_ANGLE Register

| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| IPD_ANGLE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-96. IPD\_ANGLE Register Field Descriptions

| Bit  | Field     | Type | Reset | Description   |
|------|-----------|------|-------|---|
| 31-0 | IPD_ANGLE | R    | 0h    | 32-bit value indicating measured IPD angle; $IPD\_Angle (^{\circ}) = (IPD\_ANGLE / 2^{27}) * 360^{\circ}$ |

### 7.8.5.33 ED Register (Address = 742h) [Reset = 0000000h]

ED is shown in [ED Register](#) and described in [ED Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Estimated BEMF EQ Register

图 7-121. ED Register

| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ED   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-97. ED Register Field Descriptions

| Bit  | Field | Type | Reset | Description  |
|------|-------|------|-------|--|
| 31-0 | ED    | R    | 0h    | 32-bit value indicating estimated Ed; $Ed (V) = (ED / 2^{27}) * 60 / \sqrt{3}$ |

### 7.8.5.34 EQ Register (Address = 744h) [Reset = 0000000h]

EQ is shown in [EQ Register](#) and described in [EQ Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Estimated BEMF ED Register

图 7-122. EQ Register

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EQ   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-98. EQ Register Field Descriptions

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | EQ    | R    | 0h    | 32-bit value indicating estimated Eq; Eq (V) = (EQ / 2 <sup>27</sup> ) * 60 / sqrt(3) |

#### 7.8.5.35 SPEED\_FDBK Register (Address = 752h) [Reset = 0000000h]

SPEED\_FDBK is shown in [SPEED\\_FDBK Register](#) and described in [SPEED\\_FDBK Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Speed Feedback Register

图 7-123. SPEED\_FDBK Register

|            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPEED_FDBK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-99. SPEED\_FDBK Register Field Descriptions

| Bit  | Field      | Type | Reset | Description  |
|------|------------|------|-------|--|
| 31-0 | SPEED_FDBK | R    | 0h    | 32-bit value indicating estimated rotor speed; EstimatedSpeed (Hz) = (SPEED_FDBK / 2 <sup>27</sup> ) * MAX_SPEED |

#### 7.8.5.36 THETA\_EST Register (Address = 756h) [Reset = 0000000h]

THETA\_EST is shown in [THETA\\_EST Register](#) and described in [THETA\\_EST Register Field Descriptions](#).

Return to the [ALGORITHM\\_VARIABLES Registers](#).

Estimated motor position Register

图 7-124. THETA\_EST Register

|           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| THETA_EST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

表 7-100. THETA\_EST Register Field Descriptions

| Bit  | Field     | Type | Reset | Description   |
|------|-----------|------|-------|---|
| 31-0 | THETA_EST | R    | 0h    | 32-bit value indicating estimated rotor angle; EstimatedAngle (°) = (THETA_EST / 2 <sup>27</sup> ) * 360° |

## 8 Application and Implementation

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### 备注


Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The MCF8316A device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for appliances, fans, pumps, residential and living fans, seat cooling fans, automotive fans and blowers. The following section shows a common application of the MCF8316A device.

### 8.2 Typical Applications

 8-1 shows the typical schematic of MCF8316A

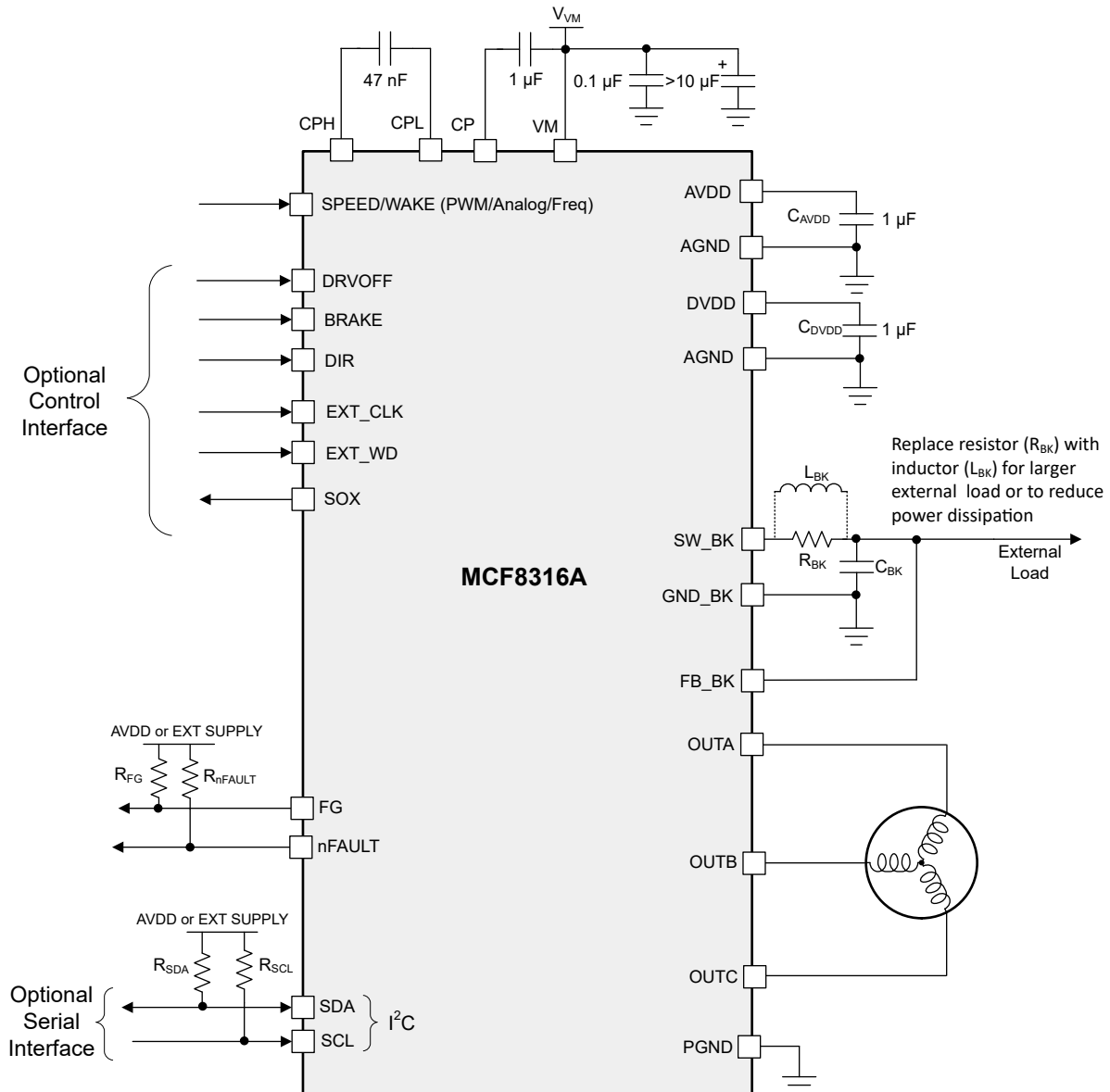


图 8-1. Primary Application Schematic

表 8-1 lists the recommended values of the external components for MCF8316A.

表 8-1. MCF8316A External Components

| COMPONENTS | PIN 1 | PIN 2 | RECOMMENDED   |
|------------|-------|-------|---|
| $C_{VM1}$  | VM    | PGND  | X5R or X7R, 0.1- $\mu$ F, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device  |
| $C_{VM2}$  | VM    | PGND  | $\geq 10$ - $\mu$ F, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device   |
| $C_{CP}$   | CP    | VM    | X5R or X7R, 16-V, 1- $\mu$ F capacitor  |
| $C_{FLY}$  | CPH   | CPL   | X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin  |
| $C_{AVDD}$ | AVDD  | AGND  | X5R or X7R, 1- $\mu$ F, $\geq 6.3$ -V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7- $\mu$ F to 1.3- $\mu$ F at 3.3-V across operating temperature. |

**表 8-1. MCF8316A External Components (continued)**

| COMPONENTS          | PIN 1               | PIN 2  | RECOMMENDED  |
|---------------------|---------------------|--------|--|
| C <sub>DVDD</sub>   | AVDD                | AGND   | X5R or X7R, 1- $\mu$ F, $\geq$ 4-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.6- $\mu$ F to 1.3- $\mu$ F at 1.5-V across operating temperature. |
| C <sub>BK</sub>     | SW_BK               | GND_BK | X5R or X7R, buck-output rated capacitor  |
| L <sub>BK</sub>     | SW_BK               | FB_BK  | Buck-output inductor   |
| R <sub>FG</sub>     | 1.8 to 5-V Supply   | FG     | 5.1-k $\Omega$ , Pull-up resistor  |
| R <sub>nFAULT</sub> | 1.8 to 5-V Supply   | nFAULT | 5.1-k $\Omega$ , Pull-up resistor  |
| R <sub>SDA</sub>    | 1.8 to 3.3-V Supply | SDA    | 5.1-k $\Omega$ , Pull-up resistor  |
| R <sub>SCL</sub>    | 1.8 to 3.3-V Supply | SCL    | 5.1-k $\Omega$ , Pull-up resistor  |

Recommended application range for MCF8316A is shown in [表 8-2](#).

**表 8-2. Recommended Application Range**

| Parameter  | Min   | Max  | Unit     |
|--|-------|------|----------|
| Motor voltage  | 4.5   | 35   | V        |
| Back-EMF constant (see <a href="#">Motor Back-EMF constant</a> ) | 0.6   | 2000 | mV/Hz    |
| Motor resistance (see <a href="#">Motor Resistance</a> )         | 0.006 | 20   | $\Omega$ |
| Motor inductance (see <a href="#">Motor Inductance</a> )         | 0.006 | 20   | mH       |
| Motor electrical speed   | -     | 1500 | Hz       |
| Peak motor phase current   | -     | 8    | A        |

Default EEPROM configuration for MCF8316A is listed in [表 8-3](#). Default values are chosen for reliable motor startup and closed loop operation. Refer to [MCF8316A tuning guide](#) which provides step by step procedure to tune a 3-phase BLDC motor in closed loop, conform to use-case and explore features in the device.

**表 8-3. Recommended Default Values**

| Address Name     | Address    | Recommended Value |
|------------------|------------|-------------------|
| ISD_CONFIG       | 0x00000080 | 0x64738C20        |
| REV_DRIVE_CONFIG | 0x00000082 | 0x28200000        |
| MOTOR_STARTUP1   | 0x00000084 | 0x0B6807D0        |
| MOTOR_STARTUP2   | 0x00000086 | 0x2306600C        |
| CLOSED_LOOP1     | 0x00000088 | 0x0D3201B5        |
| CLOSED_LOOP2     | 0x0000008A | 0x1BAD0000        |
| CLOSED_LOOP3     | 0x0000008C | 0x00000000        |
| CLOSED_LOOP4     | 0x0000008E | 0x00000000        |
| SPEED_PROFILES1  | 0x00000094 | 0x00000000        |
| SPEED_PROFILES2  | 0x00000096 | 0x00000000        |
| SPEED_PROFILES3  | 0x00000098 | 0x00000000        |
| SPEED_PROFILES4  | 0x0000009A | 0x000D0000        |
| SPEED_PROFILES5  | 0x0000009C | 0x00000000        |
| SPEED_PROFILES6  | 0x0000009E | 0x00000000        |
| FAULT_CONFIG1    | 0x00000090 | 0x3EC80106        |
| FAULT_CONFIG2    | 0x00000092 | 0x70D00888        |
| PIN_CONFIG       | 0x000000A4 | 0x00000000        |
| DEVICE_CONFIG1   | 0x000000A6 | 0x00101462        |
| DEVICE_CONFIG2   | 0x000000A8 | 0x4000F00F        |
| PERI_CONFIG1     | 0x000000AA | 0x41C01F00        |
| GD_CONFIG1       | 0x000000AC | 0x1C450100        |



表 8-3. Recommended Default Values (continued)

| Address Name | Address    | Recommended Value |
|--------------|------------|-------------------|
| GD_CONFIG2   | 0x000000AE | 0x00200000        |
| INT_ALGO_1   | 0x000000A0 | 0x2433407D        |
| INT_ALGO_2   | 0x000000A2 | 0x000001A7        |

Once the device EEPROM is programmed with the desired configuration, device can be operated stand-alone and I<sup>2</sup>C serial interface is not required anymore. Speed can be commanded using SPEED pin.

Below are the two essential parameters that are required to spin the motor in closed loop.

1. Maximum motor speed.
2. Current limit for torque PI loop.

## 8.2.1 Application Curves

### 8.2.1.1 Motor startup

图 8-2 shows the FG waveform and the phase current waveform at different motor operations.

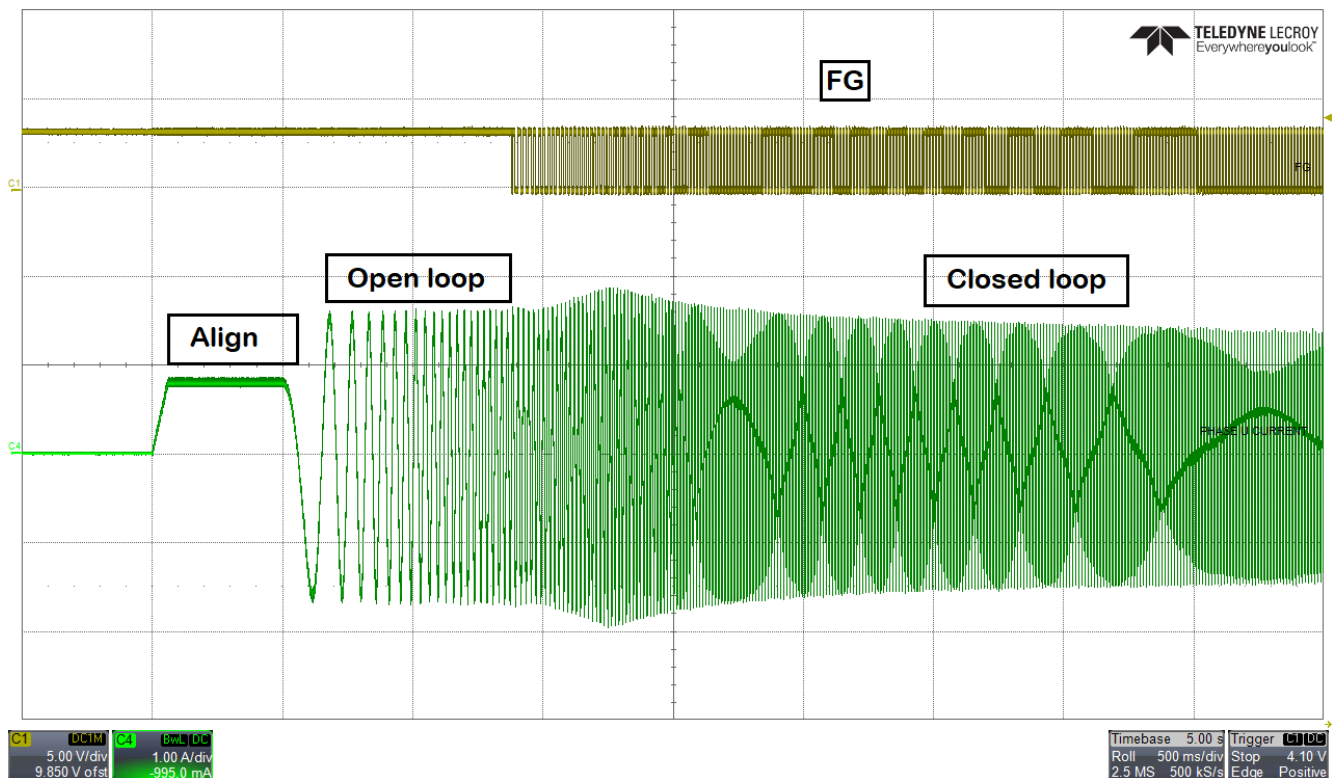


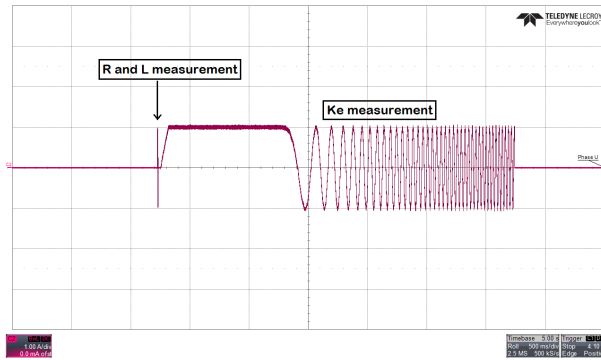
图 8-2. Motor Startup - FG and Phase current

### 8.2.1.2 MPET

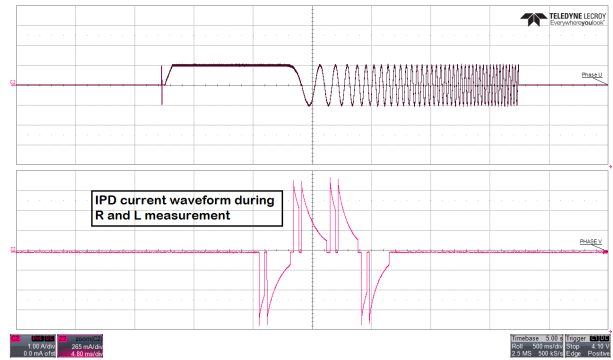
图 8-3 shows the phase current waveform during motor parameter measurement. 图 8-4 shows the IPD current waveform during R, L and Ke measurement. Bottom half of 图 8-4 shows the IPD current waveform during R and L measurement. R is measured during the rising of phase current and L is measured during the falling of phase current. After R and L measurement, motor spins in open loop. Once the speed reaches MPET open loop speed reference [MPET\_OPEN\_LOOP\_SPEED\_REF], motor is coasted. BEMF voltage of all three phases are measured and Ke is calculated.

**MCF8316A**

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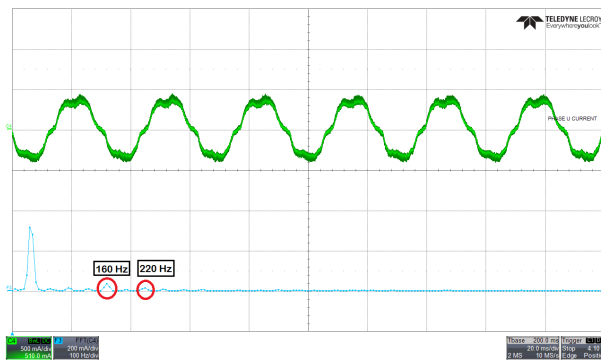
**图 8-3. MPET - Phase current**



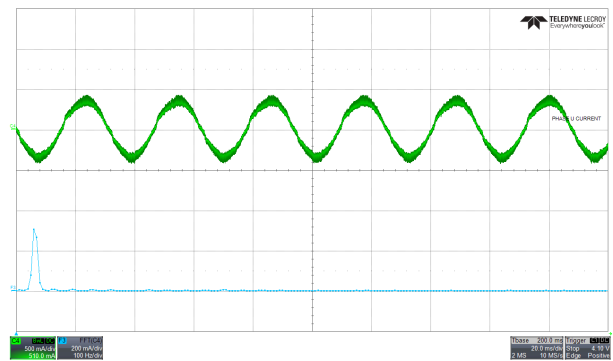
**图 8-4. IPD current waveform during R and L measurement**

**8.2.1.3 Dead time compensation**

图 8-5 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at 160 Hz and 220 Hz. 图 8-6 shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.



**图 8-5. Phase current and FFT - Dead time compensation disabled**



**图 8-6. Phase current and FFT - Dead time compensation enabled**

**8.2.1.4 Auto handoff**

图 8-7 shows the auto handoff feature in MCF8316A where the motor transitions seamlessly from open loop to closed loop.

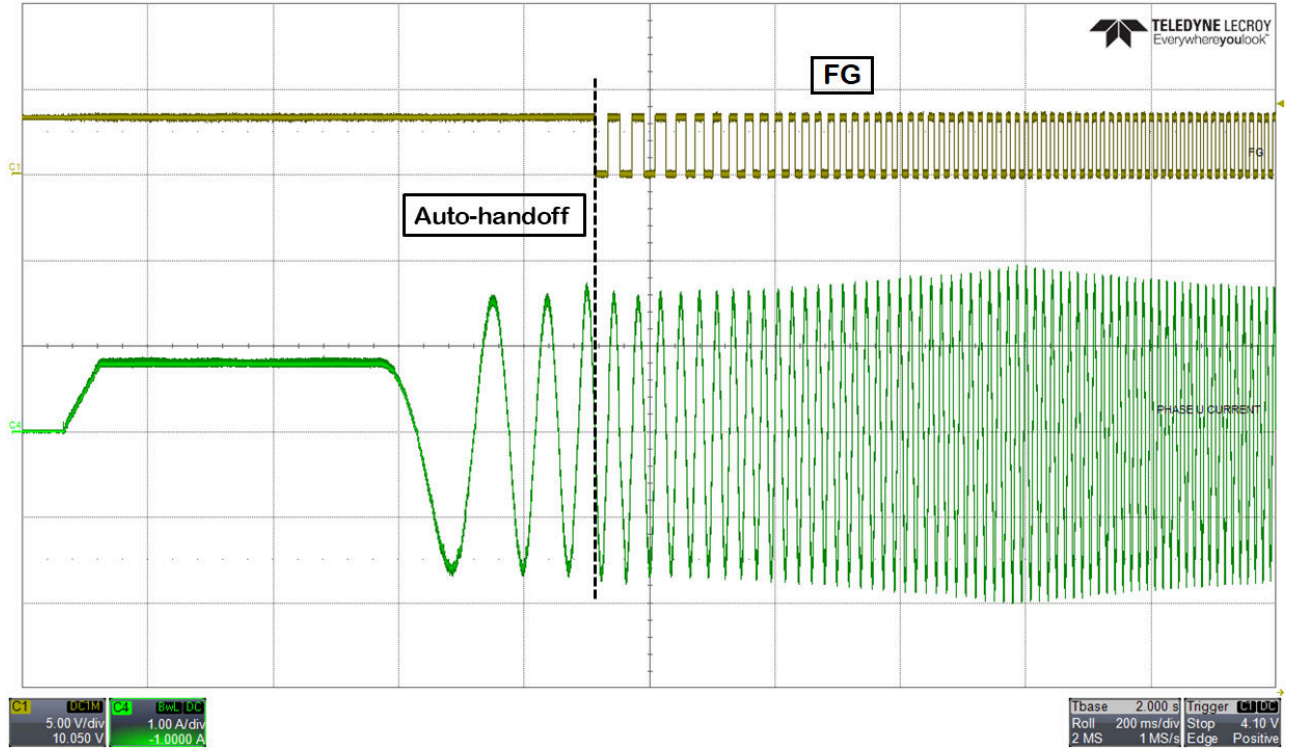


图 8-7. Auto-handoff

### 8.2.1.5 Motor stop – recirculation mode

图 8-8 shows the supply voltage and phase current waveform after stopping the motor. Recirculation mode in MCF8316A prevents the supply voltage from overshoots.

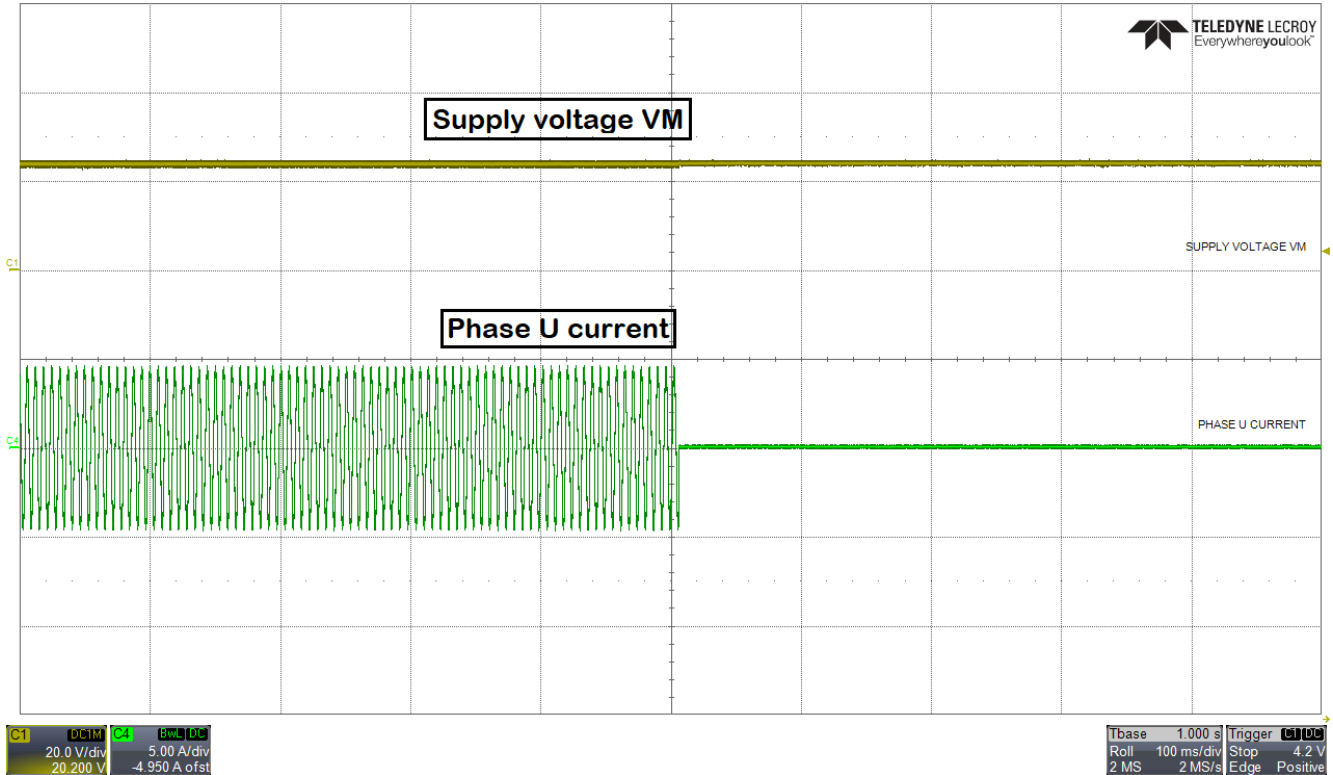


图 8-8. Motor stop - recirculation mode

### 8.2.1.6 Anti voltage surge (AVS)

When motor speed decelerates at a very high deceleration rate, mechanical energy from the motor returns to the power supply which could result in pumping up the supply voltage, VM. 图 8-9 shows overshoot in power supply voltage when AVS is disabled. Motor decelerates from 100% duty cycle to 10% duty cycle at a deceleration rate of 70,000 Hz/sec. 图 8-10 shows no overshoot in power supply voltage when AVS is enabled.

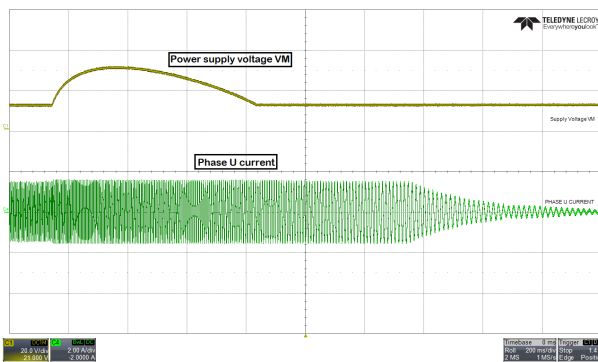


图 8-9. Power supply voltage and phase current waveform when AVS is disabled

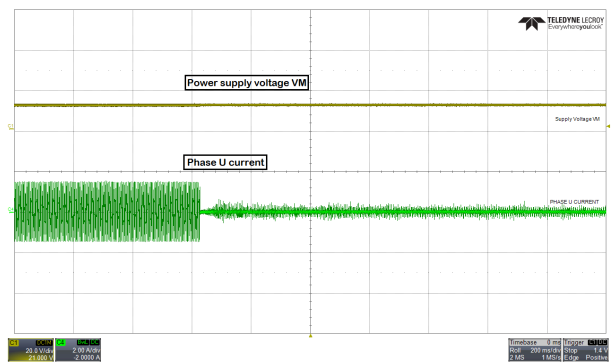


图 8-10. Power supply voltage and phase current waveform when AVS is enabled

## 9 Power Supply Recommendations

### 9.1 Bulk Capacitance

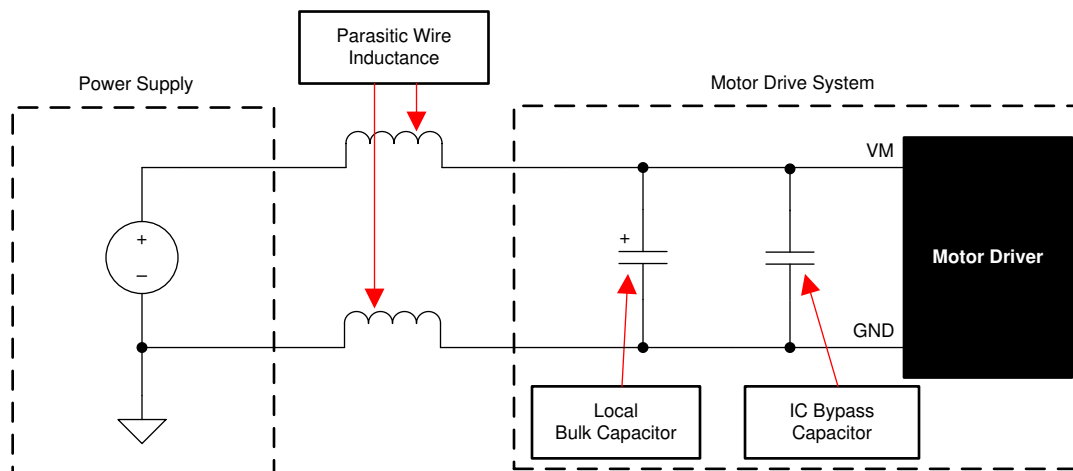
Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in VM voltage. When adequate bulk capacitance is used, the VM voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor.



**图 9-1. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

## 10 Layout

### 10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND\_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the  $I^2 \times R_{DS(on)}$  heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW\_BK and FB\_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB\_BK trace as much as possible to allow for faster load switching.

 [10-1](#) shows a layout example for the MCF8316A. Also, for layout example, refer to [MCF8316A EVM](#).

## 10.2 Layout Example

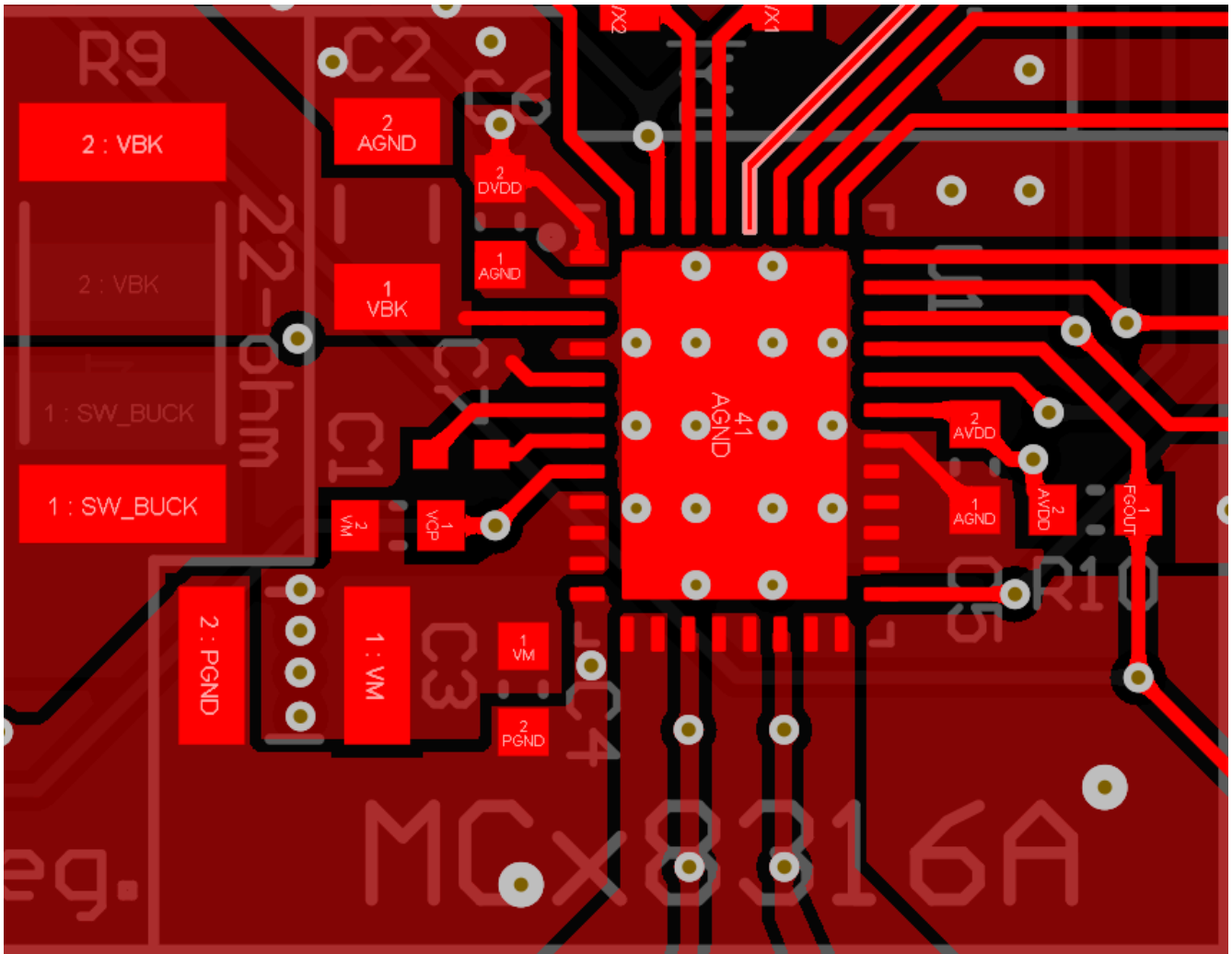


图 10-1. Recommended Layout Example

### 10.3 Thermal Considerations

The MCF8316A has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

#### 10.3.1 Power Dissipation

The power dissipated in the output FET resistance ( $R_{DS(on)}$ ) dominates power dissipation in MCF8316A.

At start-up and fault conditions, the FET current is much higher than normal operating FET current; remember to take these peak currents and their duration into consideration.

The total device power dissipation is the power dissipated in each of the three half-bridges added together along with standby power, LDO and buck regulator losses.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that  $R_{DS(on)}$  increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below in [表 10-1](#).

**表 10-1. Power Losses for MCF8316A**

| Loss type      | MCF8316A   |
|----------------|--|
| Standby power  | $P_{standby} = VM \times I_{VM\_TA}$   |
| LDO            | $P_{LDO} = (VM - V_{AVDD}) \times I_{AVDD}$ , if BUCK_PS_DIS = 1b<br>$P_{LDO} = (V_{BK} - V_{AVDD}) \times I_{AVDD}$ , if BUCK_PS_DIS = 0b |
| FET conduction | $P_{CON} = 3 \times (I_{RMS(FOC)})^2 \times R_{ds,on(TA)}$   |
| FET switching  | $P_{SW} = 3 \times I_{PK(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$   |
| Diode          | $P_{diode} = 3 \times I_{PK(FOC)} \times V_{diode} \times t_{dead} \times f_{PWM}$   |
| Buck           | $P_{BK} = 0.11 \times V_{BK} \times I_{BK}$ ( $\eta_{BK} = 90\%$ )   |



## 11 Device and Documentation Support

### 11.1 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 11.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.


### 11.4 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| MCF8316A1VRGFR   | ACTIVE        | VQFN         | RGF             | 40   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | MCF83<br>16A1V          |  |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MCF8316A1VRGFR | VQFN         | RGF             | 40   | 3000 | 330.0              | 16.4               | 5.25    | 7.25    | 1.45    | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MCF8316A1VRGFR | VQFN         | RGF             | 40   | 3000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

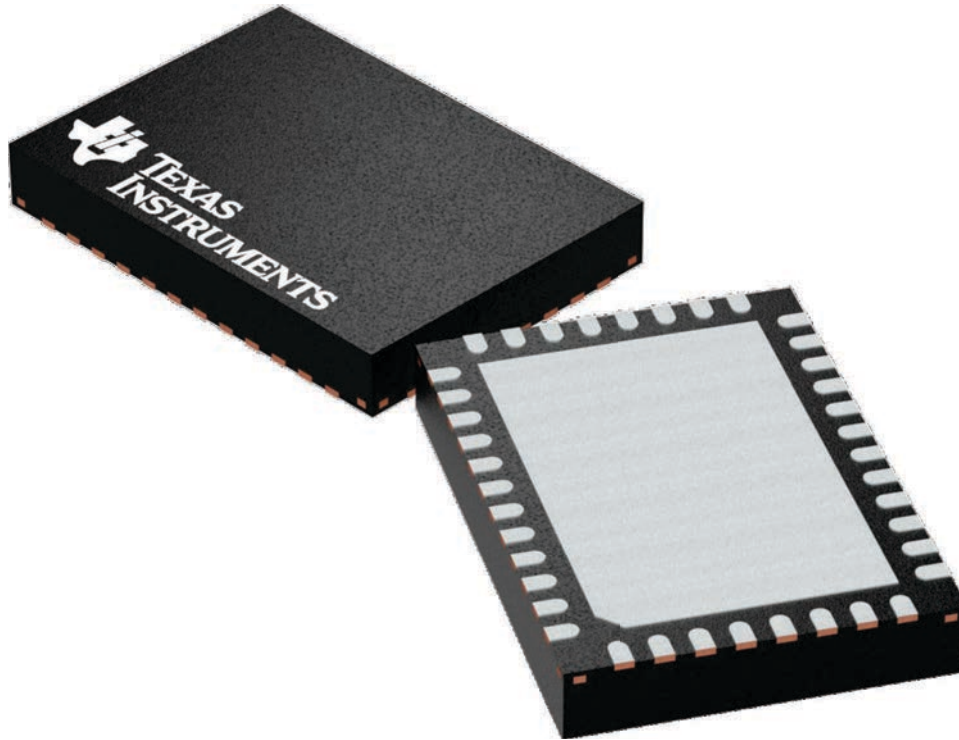
**RGF 40**

**VQFN - 1 mm max height**

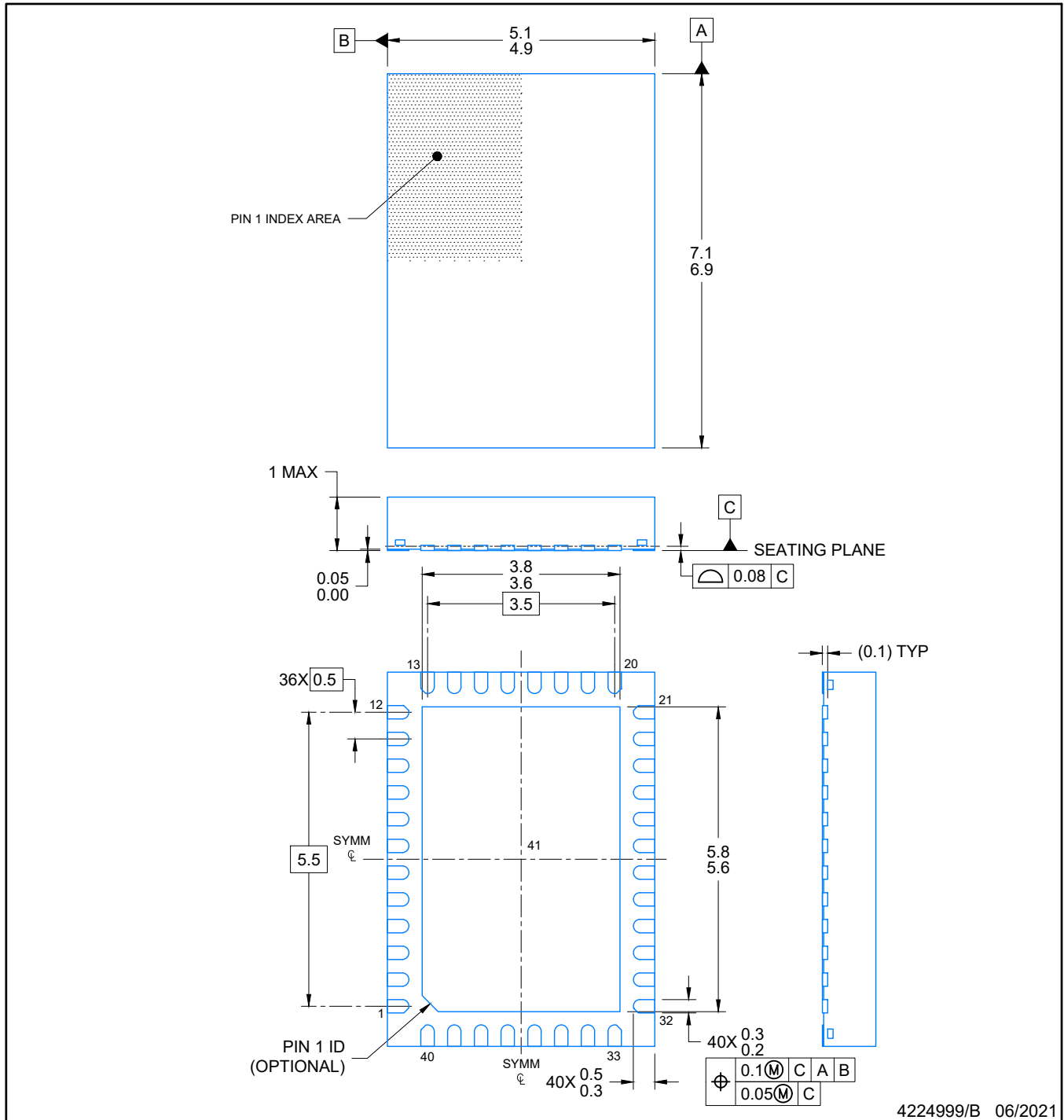
5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

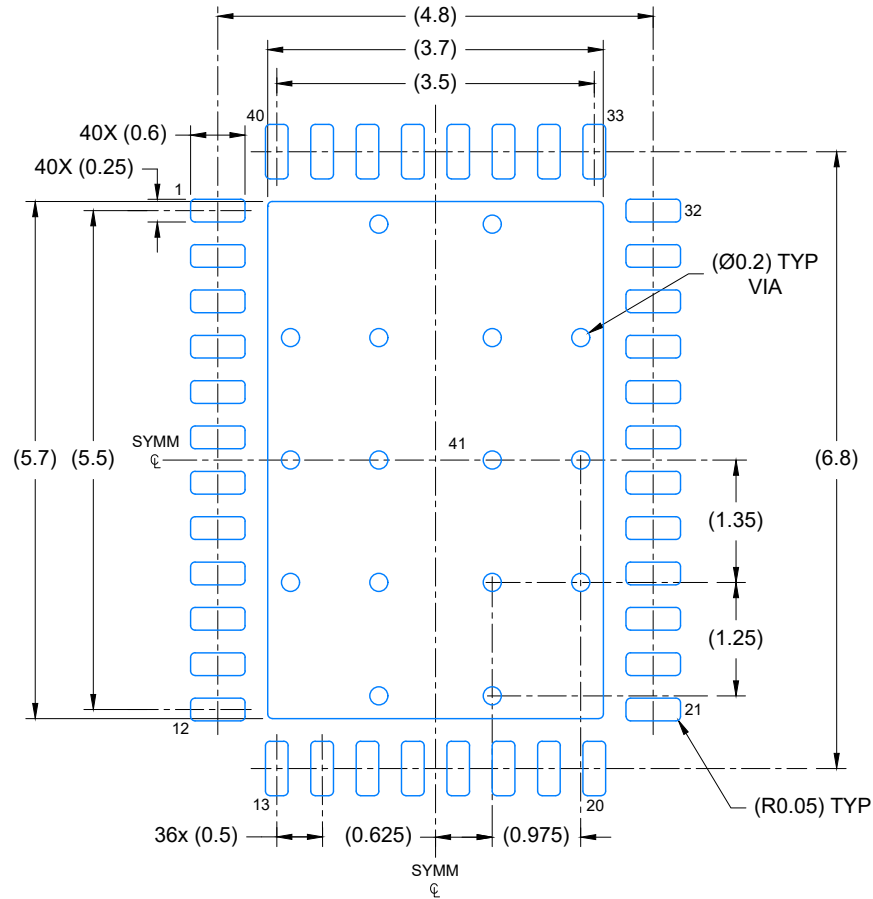


4225115/A

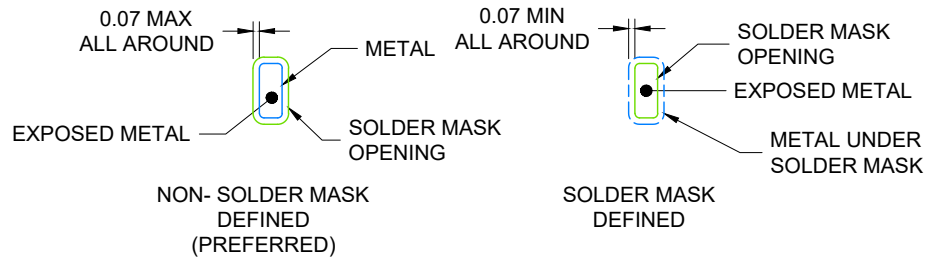


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

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NOTES: (continued)

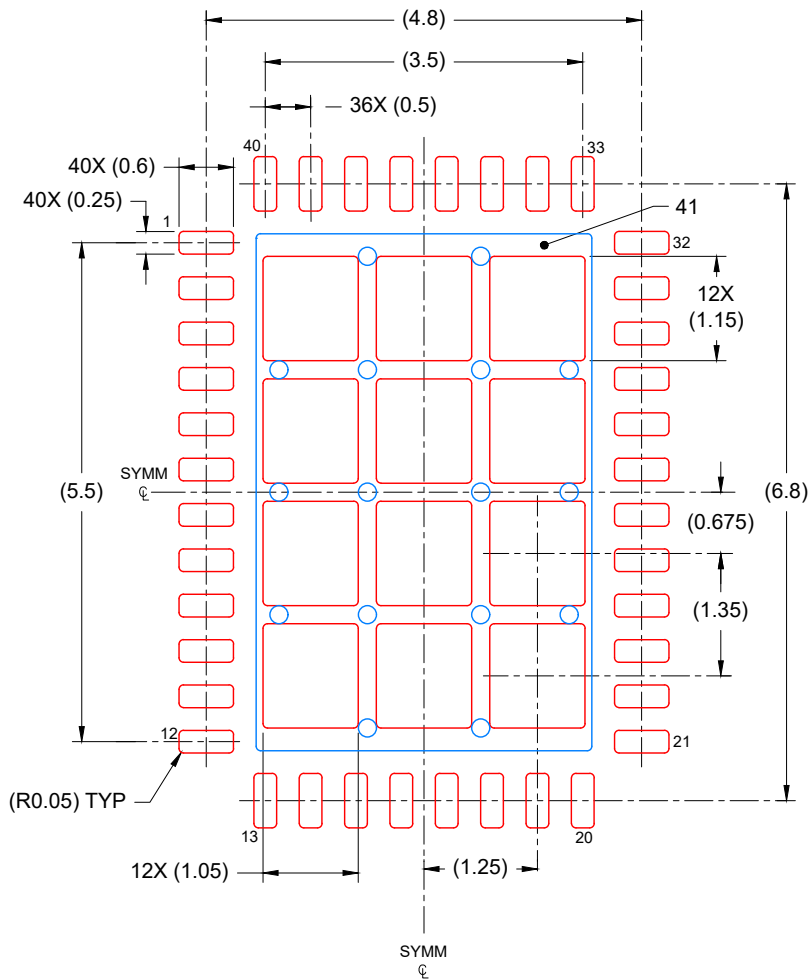
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
69% PRINTED COVERAGE BY AREA  
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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